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Educational Details

Examination/ Degree	College / University	Year of Passing
UG	JSSATE/VTU	2008
PG	JSSATE/VTU	2010
PhD	Perusing /VTU	

Publications

Journal Publications:

- B.P Aruna Rao, V Supriya a, Monisha , Penujuri Naga Sai Snehitha, Pratima P, Agnihotri" **"Modern Day Washing Machine**, International Journal of Research in Engineering, science and Management, Vol-2, Issue-11, Nov 2019
- Aruna Rao B P, Shanthi Prasad M J," Design of Programmable High Speed I/O S" Volume 6 Issue 3 , International Journal of VLSI & Signal Processing (SSRG - IJVSP) - Sep to Dec 2019,pp-18-22 ISSN: 2394 - 2584
- Aruna Rao B P, Dr. Shanthi Prasad. M.J "A Comprehensive study of Input Output [IO]functionalities of Contemporary IO" © IJEDR 2019 | Volume 7, Issue 3 | ISSN: 2321-9939
- Aruna Rao B P, Shanthi Prasad M J," Design of Programmable High Speed I/O S" Volume 6 Issue 3 - Sep to Dec 2019, ISSN: 2394 – 2584
- Maghashree V, Namratha Ganesh, Namratha Gopal, Aruna Rao B P" Village 3.0", Journal of Applied Science and Computation ,Vol.6,No 12,pp 19-26,2019, ISSN:1076-5131
- Pavithra S.P, Pooja B, Kavya V, Ashwini A, Aruna Rao, " A Survey on Raspberry PI based Reader and Smart Assistance for Visually Imapired People", | International journal of current Research vol 11, Issue, 04- pp.2794-2798, April 2019| ISSN : 0975-833X
- Aruna Rao BP, Ravi Shankar J, Dr. M. J. Shanthi Prasad, "Overview of Differential ended I/O Logic Families, International Journal of Engineering Research and Technology, ISSN: 2278-0181, Vol. 6, No. 11, pp. 1-6, Nov. 2017.

- Aruna Rao B P, Ravi Shankar J, Dr. Shanthi Prasad. M .J, "A Technical Survey of Single-ended Input/output (I/O) Logic Families & key performance parameters" International Journal of Emerging Technology and Advanced Engineering (IJETAE), UGC Approved List of Recommended Journal, Volume 8, Issue 5,pp-168-174,May 2018, ISSN 2250-2459,.

Conference Papers :

1. Aruna rao B P, Dr. Shanthi Prasad. M.J" Design and modeling of input output Functionalities of FPGA based IO block" at Global conference for advancement in technology, (GCAT-2019) Nagarjuna collage of engineering and technology, Bangalore, India 18th-20th October 2019 ISBN: 978-1-7281-3694-3

2. M.sirisha, Anitha R, Krithik P, Aruna rao B P" design and implementation of reversible computational circuits by creating libraries of basic gates using verilog HDL" at ICEECCOT 2019, 4TH International Conference on Electrical,Electronics,Communication,Computer Technologies And Optimization Techniques ,GSSS instuite of engineering and techonology for women,mysore on 13th and 14th December 2019. ISBN: 978-7281-3261-7

3. G S surabhi, Bhavana J, Madhu S, Aruna rao B P" design and implementation of 256*256 booth multipliers and its application" at ICEECCOT 2019, 4TH International Conference on Electrical,Electronics,Communication,Computer Technologies And Optimization Techniques ,GSSS instuite of engineering and techonology for women,mysore on 13th and 14th December 2019. ISBN: 978-7281-3261-7

4. Rachana S, Sahana V, Ritu Patil , Aruna rao B P" design and delay analysis of various 256-bit adders using verilog" at ICEECCOT 2019, 4TH International Conference on Electrical,Electronics,Communication,Computer Technologies And Optimization Techniques ,GSSS instuite of engineering and techonology for women,mysore on 13th and 14th December 2019. ISBN: 978-7281-3261-7

Professional Membership

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