KAMMAVARI SANGHAM

K.S.INSTITUTE OF TECHNOLOGY

(APPROVED BY A.I.C.T.E AFFILIATED TO VTU BELGAUM)

#14, RAGHUVANAHALLI, KANAKAPURA MAIN ROAD, BANGALORE-560109

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.

NAME OF THE LAB: LIC's & COMMUNICATION LAB

COURSE CODE: 17ECL48

K. S. INSTITUTE OF TECHNOLOGY

VISION

"To impart quality technical education with ethical values, employable skills and research to achieve excellence".

MISSION

- To attract and retain highly qualified, experienced & committed faculty.
- To create relevant infrastructure.
- Network with industry & premier institutions to encourage emergence of new ideas by providing research & development facilities to strive for academic excellence.
- To inculcate the professional & ethical values among young students with employable skills & knowledge acquired to transform the society.

K.S. INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

VISION :

"To achieve excellence in academics and research in Electronics & Communication Engineering to meet societal need".

MISSION:

- To impart quality technical education with the relevant technologies to produce industry ready engineers with ethical values.
- To enrich experiential learning through active involvement in professional clubs & societies.
- To promote industry-institute collaborations for research & development.

K.S. INSTITUTE OF TECHNOLOGY

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

PROGRAM EDUCATIONAL OBJECTIVES (PEO'S)

PEO1 : Excel in professional career by acquiring domain knowledge.

PEO2 : Motivation to pursue higher Education & research by adopting technological innovations by continuous learning through professional bodies and clubs.

PEO3 : To inculcate effective communication skills, team work, ethics and leadership qualities.

PROGRAM SPECIFIC OUTCOMES (PSO'S)

PSO1: Graduate should be able to understand the fundamentals in the field of Electronics & Communication and apply the same to various areas like Signal processing, embedded systems, Communication & Semiconductor technology.

PSO2: Graduate will demonstrate the ability to design, develop solutions for Problems in Electronics & Communication Engineering using hardware and software tools with social concerns.

K S INSTITUTE OF TECHNOLOGY

PROGRAM OUTCOMES (PO'S)

Engineering Graduates will be able to:

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

LINEAR ICS AND COMMUNICATION LAB

SEMESTER – IV (EC/TC)

[As per Choice Based Credit System (CBCS) Scheme]

Laboratory Code	**17ECL48**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**01Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course objectives: This laboratory course enables students to:

- Design, Demonstrate and Analyze instrumentation amplifier, filters, DAC, adder, differentiator and integrator circuits, using op-amp.
- Design, Demonstrate and Analyze multivibrators and oscillator circuits using Op-amp
- Design, Demonstrate and Analyze analog systems for AM, FM and Mixer operations. Design, Demonstrate and Analyze balance modulation and frequency synthesis. Demonstrate and Analyze pulse sampling and flat top sampling.

Laboratory Experiments:

1. Design an instrumentation amplifier of a differential mode gain of _A‘ using three amplifiers.
2. Design of RC Phase shift and Wien‘s bridge oscillators using Op-amp.
3. Design active second order Butterworth low pass and high pass filters.
4. Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
5. Design Adder, Integrator and Differentiator using Op-Amp.
6. Design of Monostable and Astable Multivibrator using 555 Timer.
7. Demonstrate Pulse sampling, flat top sampling and reconstruction.
8. Amplitude modulation using transistor/FET (Generation and detection).
9. Frequency modulation using IC 8038/2206 and demodulation.
10. Design BJT/FET Mixer.
11. DSBSC generation using Balance Modulator IC 1496/1596.
12. Frequency synthesis using PLL.

Course Outcomes:

This laboratory course enables students to:

Illustrate the pulse and flat top sampling techniques using basic circuits.

- Demonstrate addition and integration using linear ICs, and 555 timer operations to generate signals/pulses.
- Demonstrate AM and FM operations and frequency synthesis.
- Design and illustrate the operation of instrumentation amplifier, LPF, HPF, DAC and oscillators using linear IC.

Conduct of Practical Examination:

All laboratory experiments are to be included for practical examination.
Students are allowed to pick one experiment from the lot.
Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Course code 17ECL48	**Course: Linear ICs and Communication Lab**
17ECL48.1	To **analyze** Linear IC applications of DAC, adder, differentiator, and integrator using 741 IC.
17ECL48.2	Test for illustrating the pulse and flat top sampling techniques and to generate pulses using 555 IC.
17ECL48.3	Compare the frequency of oscillation to satisfy with theoretical frequency of Oscillators.
17ECL48.4	Determine the gain and frequency response characteristics of instrumentation amplifier, LPF and HPF using 741 IC.
17ECL48.5	To **evaluate** the percentage of modulation for AM and FM Techniques.

COURSE NAME- Linear ICs and Communication Lab -17ECL48

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
17ECL48.1	3	3	_	2	1	_	_	_	1	1	_	1
17ECL48.2	3	3	_	2	1	_	_	_	1	1	_	1
17ECL48.3	3	3	_	2	1	_	_	_	1	1	_	1
17ECL48.4	3	3	_	2	1	_	_	_	1	1	_	1
17ECL48.5	3	3	_	2	1	_	_	_	1	1	_	1
17ECL48	3	3	_	2	1	_	_	_	1	1	_	1

CO – PSO Mapping

CO	**PSO1**	**PSO2**
17ECL48.1	3	2
17ECL48.2	3	2
17ECL48.3	3	2
17ECL48.4	3	2
17ECL48.5	3	2
17ECL48	3	2

CONTENTS

Sl. No.	Experiment	Page no.
	Cycle - 1	
1.	RC Phase shift Oscillator and Wein's Bridge Oscillator	11-15
2.	Active low-pass and High-pass filters [II order]	16-23
3.	Digital to Analog converter	24-29
4.	Adder , Integrator and Differentiator	30-37
	Cycle-2	
5.	Astable & Monostable Multivibrators	38-43
6.	Generation and detection of Pulse sampling (PAM) and Flat top sampling	44-49
7.	Generation and detection of AM (collector modulation)	50-53
8.	BJT mixer UP/Down Conversion	54-56
	Cycle - 3	
9.	Instrumentation Amplifier	57-59
10.	FM modulation and demodulation	60-63
11.	Frequency synthesis using PLL	64-66
12.	Balanced modulator using IC 1496	67-70

EXPERIMENT: 1

RC PHASE SHIFT OSCILLATOR AND WEIN BRIDGE OSCILLATOR

AIM: To design a RC Phase Shift and Wein bridge oscillators using Op-amp for a given oscillating frequency.

a) RC PHASE SHIFT OSCILLATOR

COMPONENTS REQUIRED:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	CRO	1
3.	IC741	1
4.	Resistors: 6.8 kΩ 220kΩ 3300pF	 3 1 3
5.	Bread Board, Connecting Wires	1set

THEORY:

RC phase shift oscillator is a sinusoidal oscillator used to produce sustained well shaped sine wave oscillations. It is used for different applications such as local oscillator for synchronous receivers, musical instruments, study purposes etc. The main part of an RC phase shift oscillator is an op amp inverting amplifier with its output fed back into its input using a regenerative feedback RC filter network, hence the name RC phase shift oscillator.

By varying the capacitor, the frequency of oscillations can be varied. The feedback RC network has a phase shift of 60 degrees each, hence total phase shift provided by the three RC network is 180 degrees. The op amp is connected as inverting amplifier hence the total phase shift around the loop will be 360 degrees.

DESIGN:

Let the oscillating frequency of RC phase shift oscillator f_0=2895 Hz

$I_1 >> I_{BMAX}$

I_{BMAX}= 500nA (741)

I_1 = 50 µA

$V_0 = \pm(V_{CC}-1) \approx \pm(15-1) = \pm 14V$

$R_2 = \frac{14}{50\mu A}$ = 280KΩ (220KΩ Standard value to be used)

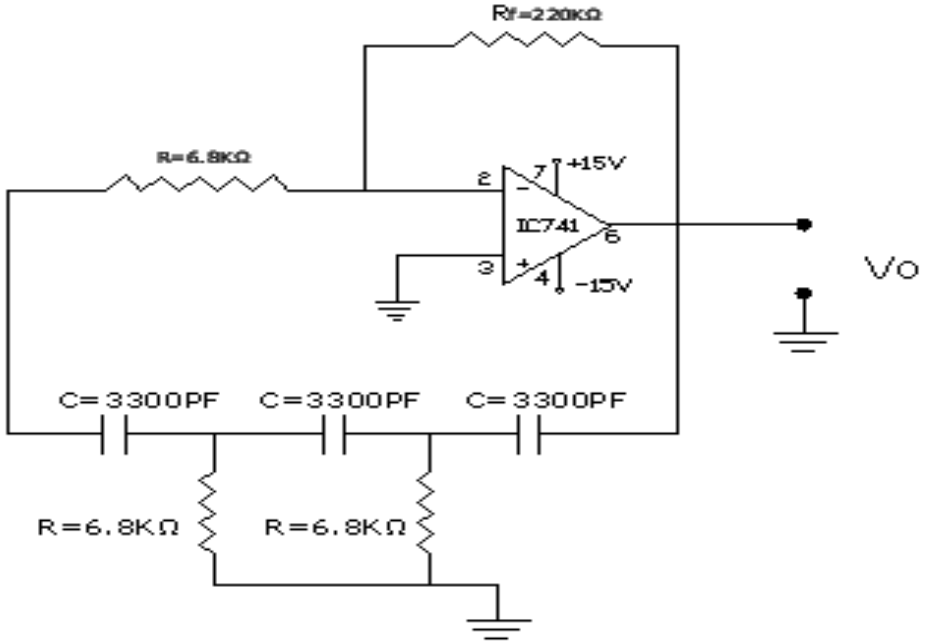
$R_1 = \frac{R_2}{A_V} = \frac{220K\Omega}{29}$ =7.6 KΩ (6.8KΩ Standard value to be used)

Select R = R_1 = 6.8 KΩ

$$C = \frac{1}{2\pi Rc\sqrt{6}} = \frac{1}{2\pi x\ 6.8\ x\ 10^3 x\ 2895\ x\sqrt{6}}$$

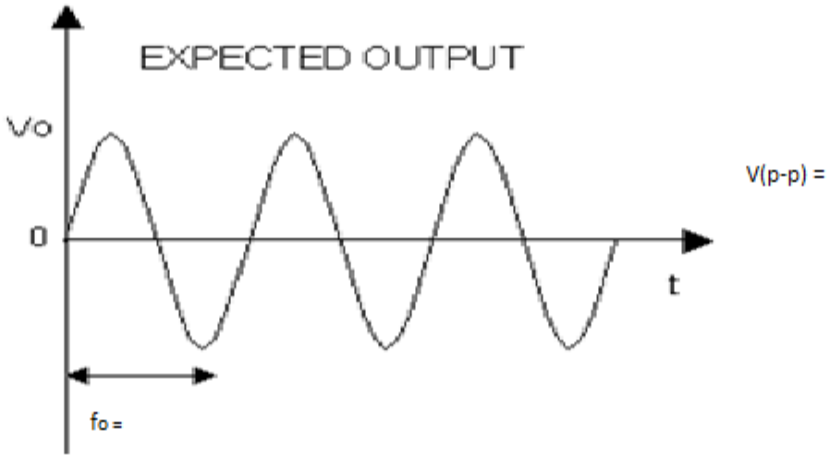
= 3.3 x 10^{-9}F =3300 pF .(Standard value)

RC Phase Shift Oscillator



PROCEDURE:

1. Rig up the circuit as shown in circuit diagram.
2. Apply the +15V and -15V voltages to the IC741.
3. Observe the output waveform at pin no. 6 .
4. Note down the frequency and amplitude of the output waveform and compare it with theoretical value.



Observations

Output Voltage Vo=_____ at fo=_____

b) WEIN BRIDGE OSCILLATOR

COMPONENTS REQUIREMENT:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	CRO	1
3.	IC741	1
4.	Resistors: 0.01µF 1KΩ 10kΩ Pot	 2 3 1
5.	Bread Board, Connecting Wires	1set

THEORY:

Because of its simplicity & stability, one of the most commonly used audio frequency oscillators is the Wein bridge. Figure shows the Wein bridge oscillator in which the Wein bridge circuit is connected between the amplifiers input terminal & the output terminal. The bridge has a series RC network in one arm & a parallel RC network in the adjoining arm. In the remaining two arms of the bridge, resistors R_1&$R_f$are connected as shown in figure.

The phase angle criterion for oscillation is that the total phase shift around the circuit must be 0o. This condition occurs only when the bridge is balanced, that is, at resonance. The frequency of oscillation f0 is exactly the resonant frequency of the balanced Wein Bridge & is given by

$$f_0 = \frac{1}{2\pi RC}$$

DESIGN:

Let the frequency of Wein's bridge oscillator =15 KHz

Select
$C_1 = C_2 = C = 0.01\mu F$

$$R = \frac{1}{2\pi fC} = \frac{1}{2\pi x\ 15khzx\ \ 0.01\ x10^{-6}}$$

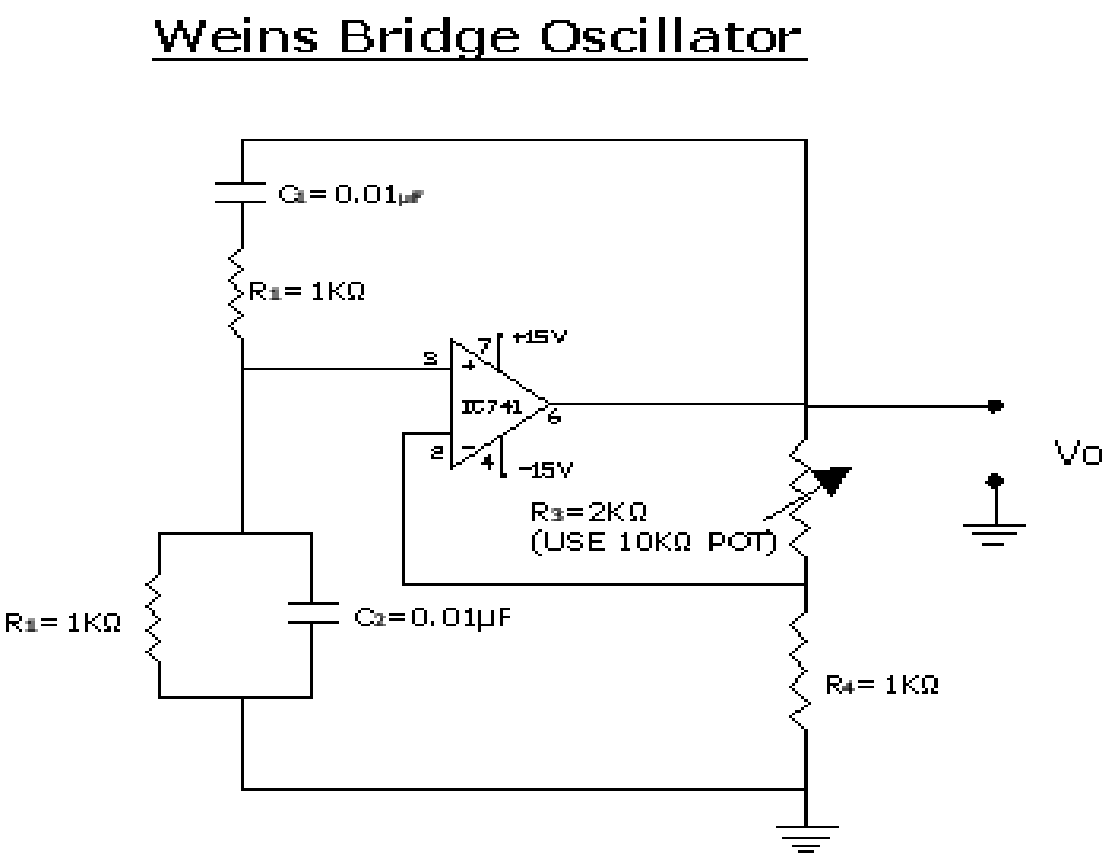
= 1.06KΩ (1kΩ Standard value to be used)

$R_1 = R_2 = R = 1K\Omega$

Let $R_4 = 1\ K\Omega$

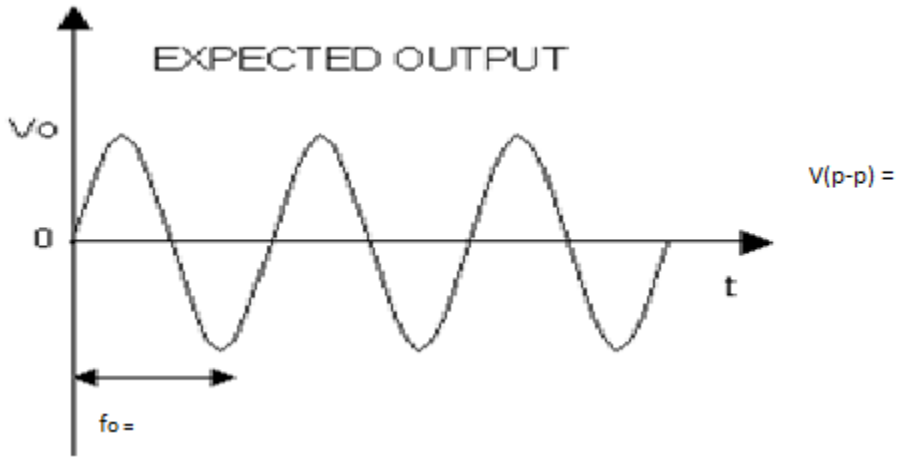
$A_V = 3$, $R_3 = 2R_4 = 2\ X\ 1K\Omega = 2K\Omega$

Use 10KΩ potentiometer



PROCEDURE:

1. Rig up the circuit as shown in circuit diagram.
2. Apply the +15V and -15V voltages to the IC741.
3. Observe the output waveform at pin no. 6 on CRO.
4. Note down the frequency and amplitude of the output and compare it with theoretical value.



Observation

Output Voltage Vo=_____ at fo=_____

RESULT :

RC Phase Shift Oscillator	(Theoretical) Frequency f_0= 2895 Hz	(Practical) Frequency f_0=
Wein Bridge Oscillator	(Theoretical) Frequency f_0=15 KHz	Practical) Frequency f_0=

EXPERIMENT: 2
ACTIVE LOW-PASS AND HIGH-PASS FILTERS [II ORDER]

AIM: To design and conduct an experiment on active second order Butterworth low pass filter and High pass filter for a given cut-off frequency and to plot the frequency response .

a) SECOND ORDER ACTIVE LOW-PASS FILTER

COMPONENTS REQUIRED:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	Function Generator	1
3.	CRO	1
4.	IC741	1
5.	Resistors: 68KΩ 150KΩ 3300pF 1600pF	 2 1 1 1
6.	Bread Board, Connecting Wires	1set

THEORY:

A filter is a circuit that is designed to pass a specified band of Frequencies while attenuating all signals outside this band. Filter network may be either active or passive.
Passive filter networks contain only resistors, inductors and capacitors.
Active filter networks contain transistors or op-amps plus resistors & capacitors.

There are four types of filters

- Low pass filters
- High pass filters
- Band pass filters
- Band stop filters

LOW PASS FILTER:

A low-pass filter is a circuit that has a constant output voltage from dc up to a cutoff frequency f_c. As the frequency increases above f_c, the output voltage is attenuated (decreases).
Figure shows a first order low-pass Butterworth filter that uses an RC network for filtering. And the op-amp is used in the non-inverting configuration; hence it does not load down the RC network. Resistors R_1& R_F determine the gain of the filter.

I already said the low-pass filter has a constant gain A_F from 0 Hz to the high cutoff frequency f_c. At f_c the gain is 0.707 A_F and after fc it decreases at a constant rate with an increase in frequency. That is, When the frequency is increased tenfold (one decade), the voltage gain is divide by 10.In other words, the gain decreases 20dB(=20 log 10) each time the frequency is increased by 10.Hence the rate at which the gain rolls off after f_c is 20dB/decade by 10.Where octave signifies a two fold increase in frequency. The frequency $f=f_c$ is called the cut off frequency because the gain of the filter at this frequency is done by 3 dB (=20 log 0.707) from 0 Hz.other equivalent terms for cut off frequency are-3dB frequency, break frequency, or corner frequency.

DESIGN:

Second order Butterworth low pass filter for a given cut-off frequency of 1KHz.

Design:

$R_1 + R_2 = \frac{70mV}{I_{B(max)}} = \frac{70mV}{500nA}$

$= 140\ K\Omega$

$R_1 = R_2 = 70K\Omega$ (use 68 KΩ standard value)

$R_3 = R_1 + R_2 = 136K\Omega$ (use 150kΩ standard value)

$X_{C1} = \sqrt{2}\ R_2$ at f_C

$C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi X\ 1kHz X \sqrt{2} X\ 68\ k\Omega}$

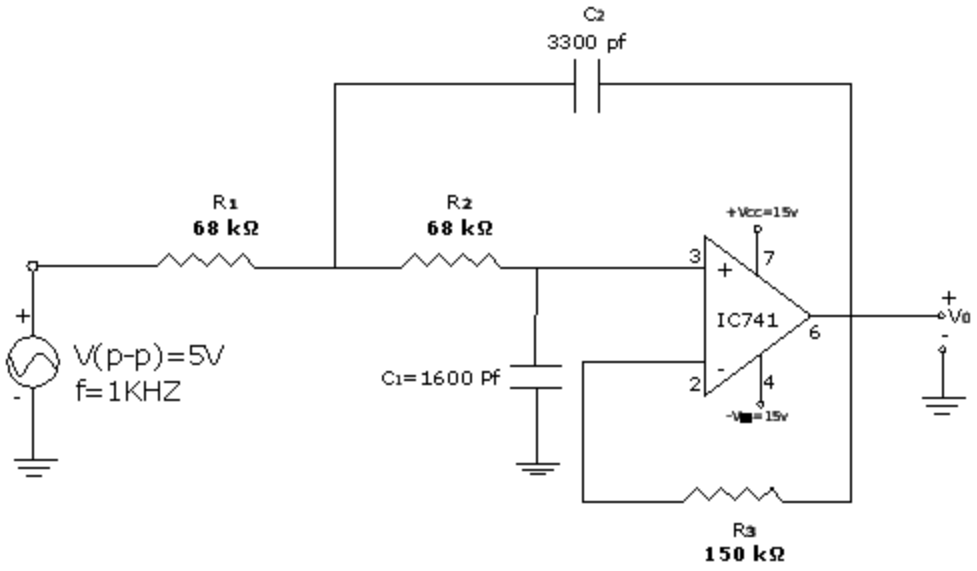
$C_1 = 1655$ pF(use 1600 pF standard value)

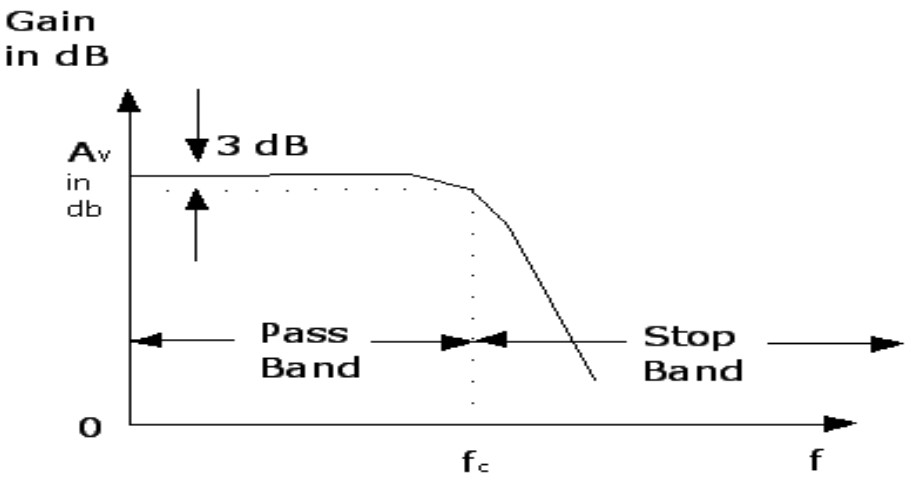
$C_2 = 2C_1 = 2 \times 1600$ pF $= 3200$ pF (use 3300 pF standard value)

PROCEDURE:

1. Rig up the circuit as shown in circuit diagram.
2. Initially keep the Input voltage $V_{in} = 5V$ constant at a frequency of 1KHz and observe the waveform.
3. Keeping the input voltage constant at 5V, vary the frequency of the signal generator in steps of 100Hz and note down the corresponding output voltage on CRO.
4. Plot the graph using semi log sheet taking frequencies along x-axis and gain in dB along y-axis.
5. Find the practical value of f_c from the graph.
6. Compare theoretical and practical values.

Second Order Low Pass Filter





Expected Curve

TABULATION:

Input Voltage V_i=5 V constant

Frequency Hz	O/P Voltage V_o	Gain=Vo/Vi	Gain in dB=$20\log_{10}(V_o/V_i)$
100 200 300 400 500 600 700 800 900 1k 2k 3k 4k 5k 10k			

Observation

Vo=_____ at fc= _____

Low pass filter	Cut off frequency f_c= (Theoretical)	Cut off frequency f_c= (Practical)

RESULT:

The maximum o/p voltage is _____
Thus , characteristics of low pass filter is verified.

b) SECOND ORDER ACTIVE HIGH-PASS FILTERS

COMPONENTS REQUIREMENT:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	Function Generator	1
3.	CRO	1
4.	IC741	1
5.	Resistors: 68KΩ 150KΩ 0.001μF	 1 2 2
6.	Bread Board, Connecting Wires	1set

THEORY:

High pass filters attenuate the output voltage for all frequencies below the cut-off frequency f_c. Above f_c, the magnitude of the output voltage is constant. The range of frequencies that are transmitted is known as the pass band. The range of frequencies that are attenuated is known as the stop band.

High pass filters are often formed simply by interchanging frequency determining resistors is formed and capacitors in low-pass filters. That is first-order high-pass filter is formed from a first order low-pass type by interchanging components R & C.

Figure shows a first order high pass Butter worth filter with a low cut off frequency of f_c. This is the frequency at which the magnitude of the gain is a 0.707 times its pass band value. Obviously, all frequencies higher that f_c are pass band frequencies, with the highest frequency determined by the closed-loop bandwidth of the op-amp.

DESIGN:

Second order Butterworth High pass filter for a given cut-off frequency of 1.5 KHz

$I_{B(MAX)}$ = 500nA

$R_2 = \frac{70mV}{500nA} = 140K\Omega$ (use 150kΩ standard value)

$R_1 = \frac{R_2}{2} = 70K\Omega$(use 68kΩ standard value)

$R_2 = \sqrt{2}\,C_1\ at f_c = 1.5KHz$

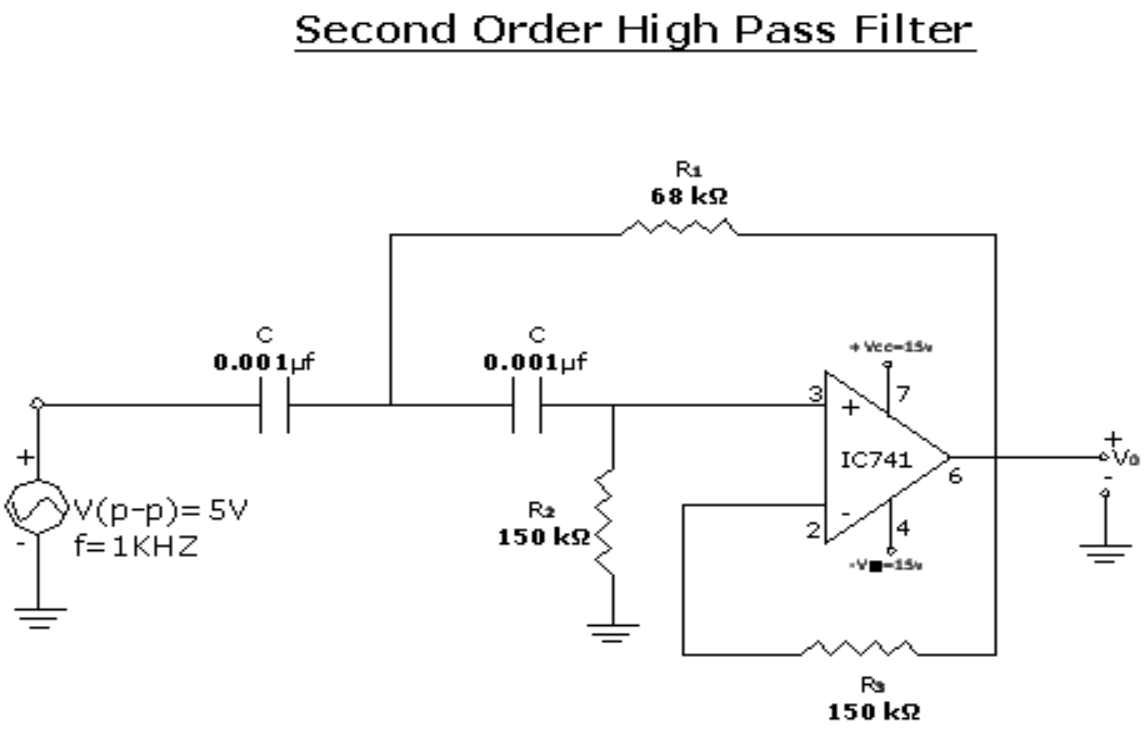
$C_2 = \frac{\sqrt{2}}{2\pi f_c R_2}$

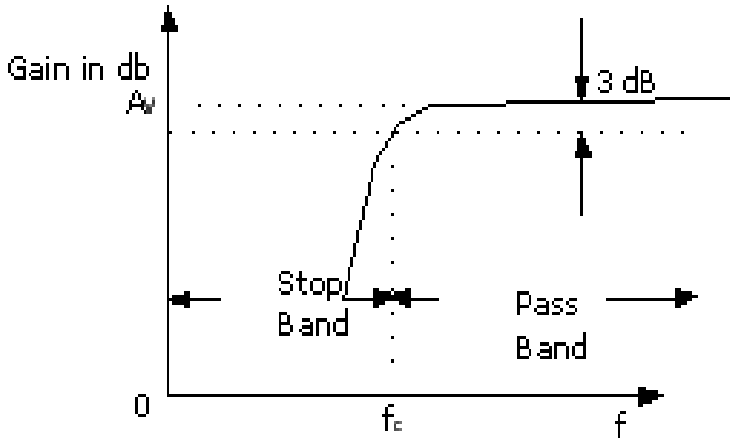
$C_2=\frac{\sqrt{2}}{2\pi x\ 1.5\ x10^3 x\ 150\ \ x10^3}$

=1nF
= 0.001μF

PROCEDURE:

1. Rig up the circuit as shown in circuit diagram.
2. Initially keep the Input voltage V_{in}= 5V constant at a frequency of 1.5KHz.
3. Vary the frequency of the signal generator in steps of 100Hz keeping input voltage constant at 5V and note down the corresponding output waveform on CRO.
4. Plot the graph using semi log sheet taking frequencies along x-axis and gain in dB along y-axis.
5. Find the practical value of f_c from the graph.
6. Compare theoretical and practical values.





Expected Frequency Response Curve

TABULATION:

Input Voltage V_{in}=5 V

Frequency Hz	O/P Voltage V_o	Gain=V_o/V_i	Gain in dB=$20\log_{10}(V_o/V_i)$
100			
200			
300			
400			
500			
600			
700			
800			
900			
1k			
1.5k			
2k			
3k			
4k			
5k			
10k			
20k			
30k			

Observation

Vo=_____ at fc= _____

High pass filter	Cut off frequency f_c= (Theoretical)	Cut off frequency f_c= (Practical)

RESULT:

The maximum o/p voltage is _____
Thus, characteristics of high pass filter is verified

EXPERIMENT: 3

DIGITAL TO ANALOG CONVERTER

AIM: To design and construct a 4 – bit R-2R Op-amp digital to analog converter using 4-bit binary input from toggle switches and Mod-16 Counter.

a) DIGITAL TO ANALOG CONVERTER USING TOGGLE SWITCHES

COMPONENTS REQUIRED:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	IC741	1
3.	Resistors: 1KΩ 2.2KΩ 3.3KΩ	 3 6 1
4.	Bread Board, Connecting Wires	1set
5.	Multi-meter	1

THEORY:

The D/A converter converts digital or binary data into its equivalent analog value. In R-2R ladder D/A converter, resistors of only two values, i.e. R and 2R are used. Hence, it is suitable for integrated circuit fabrication. The principle of operation of a ladder type network for 4-bit D/A conversion is shown in circuit diagram, with 4-bit binary input, b_1 b_2 b_3 b_4, analog outputs V_o and one terminating resistor 2R.

DESIGN: for 0 .5 volts step size

To generate analog signals from binary BCD input for a given step voltage with LSB = 0.5V
The full-scale analog output required for a DAC is 5V. The digital word available is at 4 bits.

$$V_0 = \frac{V_R [2^0B_0 + 2^1B_1 + 2^2B_2 + 2^3B_3]}{2^n}$$

Where B_0 ,B_1 ,B_2 ,B_3 are Binary Inputs

Design for full scale output voltage of 5 Volts

$$V0 = \frac{V_R [2^0B_0 + 2^1B_1 + 2^2B_2 + 2^3B_3]}{}$$

2^n

When all bits are high is $B_0\ B_1\ B_2\ B_3$ = 5V [Maximum]

Then V_0 = 5V

$$5\ V = \frac{V_R\ [2^0+2^1+2^2+2^3]}{2^4}$$

$$5V = \frac{V_R}{16}\ X\ 15$$

$$V_R = \frac{5X16}{15} = 5.33V$$

V_R = 5.33V

PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Apply Binary inputs from 0000 to 1111 and note down the corresponding output voltage using multi-meter.
3. Compare these output voltage values with theoretical values.
4. Plot the graph of Vo(Practical) verses binary inputs.

Tabulation

Binary Inputs	Analog o/p Voltage (V)	
$B_3\ B_2\ B_1\ B_0$	Theoretical V_0	Practical Vo
0 0 0 0	-0	
0 0 0 1	-0.33	
0 0 1 0	-0.66	
0 0 1 1	-0.99	
0 1 0 0	-1.32	
0 1 0 1	-1.67	
0 1 1 0	-2	
0 1 1 1	-2.33	
1 0 0 0	-2.66	
1 0 0 1	-2.99	
1 0 1 0	-3.32	
1 0 1 1	-3.67	
1 1 0 0	-4	
1 1 0 1	-4.33	
1 1 1 0	-4.66	
1 1 1 1	-4.99 (5V)	

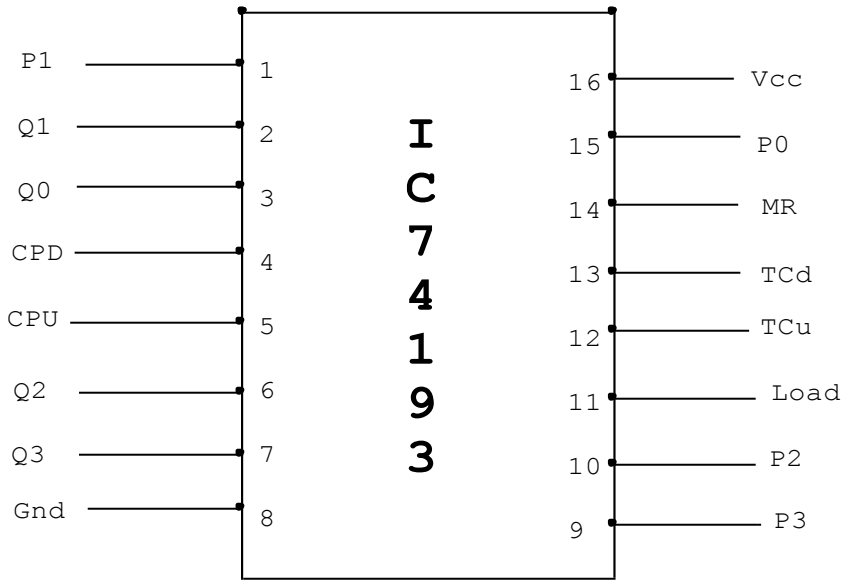
b) DIGITAL TO ANALOG CONVERTER USING MOD-16 COUNTER

AIM: To design and conduct a 4 – bit R-2R Op-amp digital to analog converter by generating digital inputs using MOD-16 counter.

COMPONENTS REQUIREMENT:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	IC741	1
3	IC74193	1
4.	Resistors: 1KΩ 2.2KΩ 3.3KΩ	 3 6 1
5.	Bread Board, Connecting Wires	1set
6.	Multi-meter	1
7.	IC Trainer Kit	1

Pin Details of IC74193:



IC74193 Binary Up/Down Presettable Counter:

PIN Name	Description
P0 – P3	Parallel data inputs
Q0 – Q3	Outputs
MR	Master Reset (clr)
Load	Asynchronous parallel load (Active low)

Use of 74193 as up counter:
Truth table

Clock	Q_3	Q_2	Q_1	Q_0
↓	0	0	0	0
↓	0	0	0	1
↓	0	0	1	0
↓	0	0	1	1
↓	0	1	0	0
↓	0	1	0	1
↓	0	1	1	0
↓	0	1	1	1
↓	1	0	0	0
↓	1	0	0	1
↓	1	0	1	0
↓	1	0	1	1
↓	1	1	0	0
↓	1	1	0	1
↓	1	1	1	0
↓	1	1	1	1

TABULATION

Binary Inputs	Analog output voltage Vo(V)
B_3 B_2 B_1 B_0	
0 0 0 0	
0 0 0 1	
0 0 1 0	
0 0 1 1	
0 1 0 0	
0 1 0 1	
0 1 1 0	
0 1 1 1	
1 0 0 0	
1 0 0 1	
1 0 1 0	
1 0 1 1	
1 1 0 0	
1 1 0 1	
1 1 1 0	
1 1 1 1	

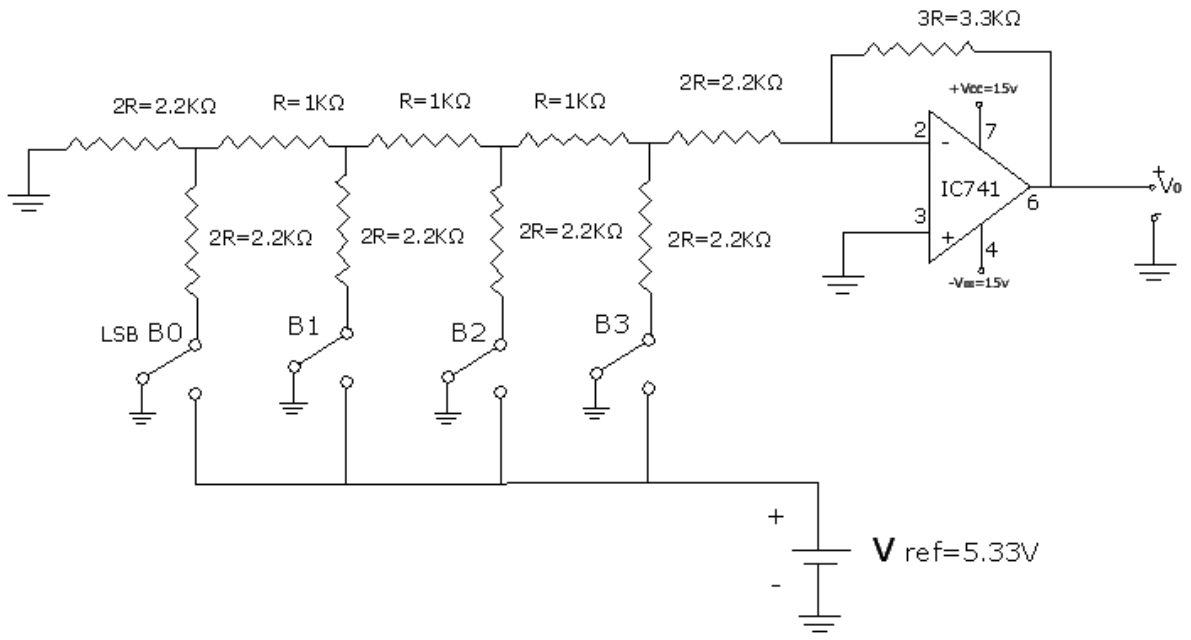
PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Apply Binary inputs from 0000 to 1111 from the counter
3. Measure the output voltage using multi-meter.
4. Plot the graph of Vo(Practical) verses binary inputs.

RESULT:

Full scale o/p voltage	Theoretical Analog o/p voltage(Full Scale)	Practical Analog o/p voltage using toggle switch(Full Scale)	Practical Analog O/P Voltage using MOD 16 counter(Full Scale)

R-2R DAC using Operational Amplifier



EXPERIMENT: 4

ADDER, INTEGRATOR AND DIFFERENTIATOR

AIM: To design an ADDER circuit using op-amp 741 and verify its working demonstrate an experiment for Adder, Differentiator and Integrator.

a) ADDER

COMPONENTS REQUIRED:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	Function Generator	1
3.	CRO	1
4.	IC741	1
5.	Resistors: 6.8KΩ 22KΩ	 1 3
6.	Bread Board, Connecting Wires	1set

THEORY:

Adder circuit that amplifies the sum of two or more inputs. This is essentially an inverting amplifier with two input terminals and two input resistors. As with other inverting amplifier, the inverting terminal of op-amp behaves as a virtual ground.

DESIGN:

Let input voltage V_i = 1.1V
In an inverting amplifier V_o=- (aV_1+bV_2)
Where a = b = 1
I_{Bmax}= 500 nA, Let = V_1= V_2=1.1V
I_f =100 I_{Bmax}= 100 X 500 nA = 50 µA
V_o = - [aV_1+bV_2]

Let a=b=1 for adder

$R_1=\frac{V_i}{I_f}=\frac{1.1}{50\mu A}=22\ K\Omega$

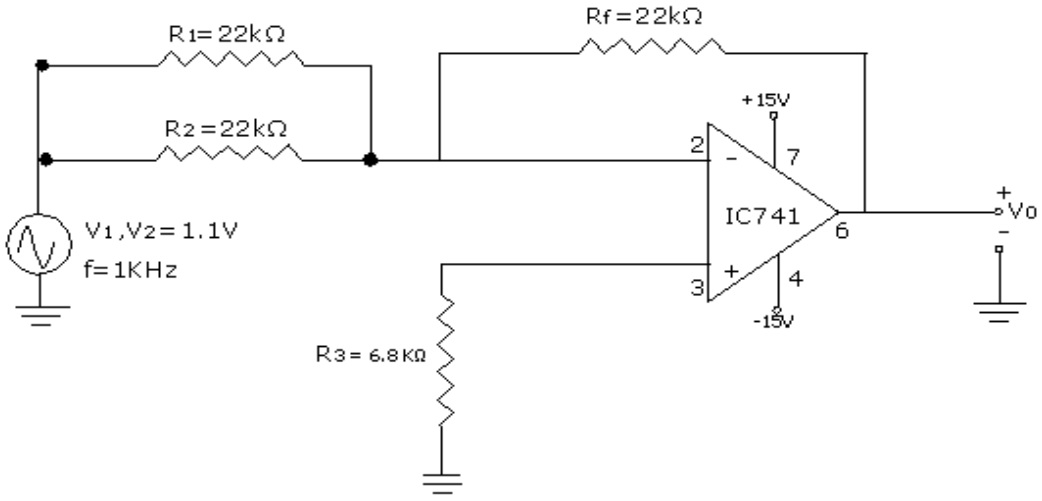
R_1= R_2=R_f=22 $K\Omega$ (std value)

R_3= $R_1 \| R_2 \| R_f$=7.333$K\Omega$ use 6.8kΩ

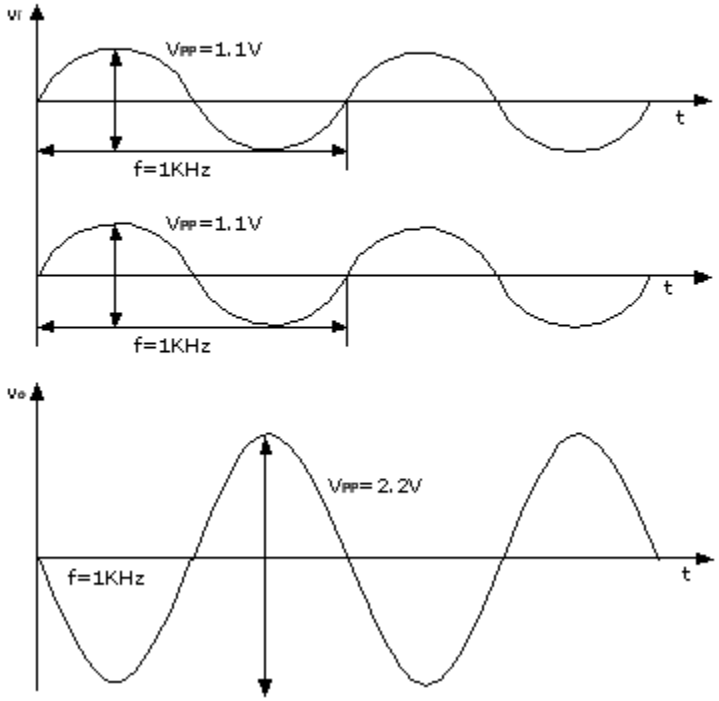
$V_0=-[V_1+V_2]=V_1 = V_2=1.1V$

ADDER

Inverting summing amplifier



ADDER WAVEFORMS



PROCEDURE:

1. Connections are made as shown in the circuit diagram of fig1.
2. Set the power supply to +15V and -15V.
3. Apply ac input sine wave of amplitude of $V_1=V_2=1.1V$ and a frequency of 1kHz.
4. Observe the input and output using CRO.
5. Plot the input and output waveforms.

Observation

V_1 =
V_2 =
V_o=

RESULT:

Theoretical	**Practical**
V_o= 2.2V	V_o=

b) DIFFERENTIATOR AND INTEGRATOR

AIM: Design a differentiator and integrator using operational amplifier 741 and verify its working.

COMPONENTS REQUIRED FOR DIFFERENTIATOR:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	Function Generator	1
3.	CRO	1
4.	IC741	1
5.	Resistors: 10KΩ 470KΩ 0. 05μF	 2 1 1
6.	Bread Board, Connecting Wires	1set

THEORY:

A differentiation and integration can be performed by op-amp circuits. A differentiating circuit is employed to produce output amplitude proportional to the rate of change of an input voltage. The output of an integrating circuit must be proportional to the area under each half cycle of the input waveform. Op-amp differentiating and integrating circuits are inverting amplifiers. Differentiating circuits are usually designed to respond to triangular and rectangular input waveforms. While integrating circuits are most often designed to produce a triangular wave output from a square wave input.Both circuits have frequency limitations when processing sine waves.

DIFFERENTIATOR DESIGN:

Let V_o=5V, Select a ramp input with amplitude 1V for a frequency of 5KHz

$I_1 >> I_{B(MAX)}$

Let$I_{1=}$500µA

$$R_2 = \frac{V_o}{I_1} = \frac{5V}{500\mu A} = 10\text{K}\Omega \text{ (Std. Value)}$$

$$C_{1=}\frac{I_1 x\, \Delta t}{\Delta v} = \frac{500\mu AX\ \ 100\ \mu s}{1V}$$

=0.05 µF (Std. Value)

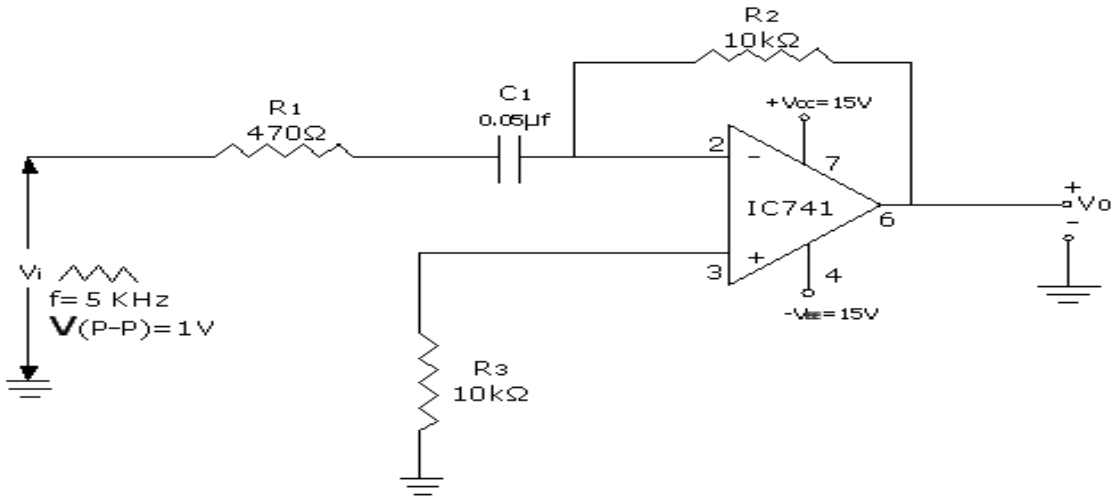
$$R_1 = \frac{R_2}{20} = \frac{10\text{k}\Omega}{20}$$

= 500Ω(use 470 Ω std value)

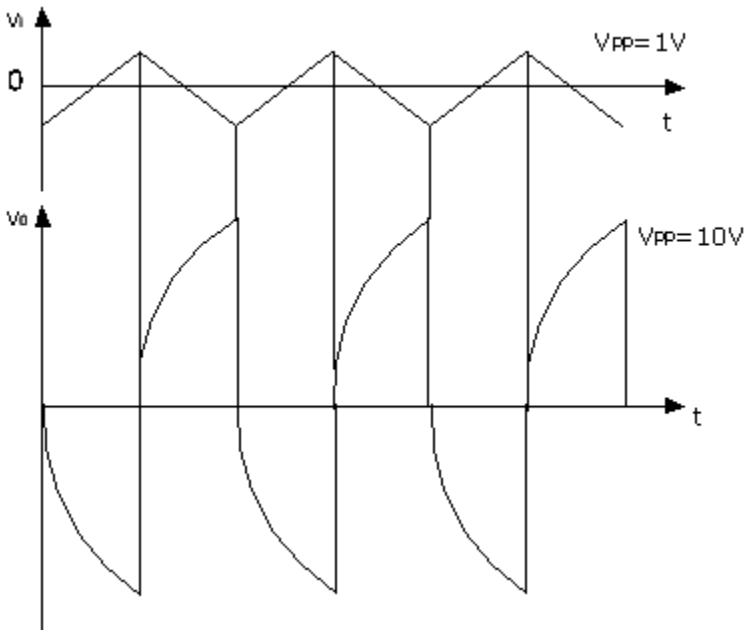
$R_3 = R_2$=10K Ω

$V_{CC} \geq \pm (V_0 + 3V) = \pm (5V + 3V)$
$\geq \pm 8V$

Differentiator



Differentiator out put wave form for Ramp wave input



PROCEDURE:

1. Connections are made as shown in the circuit diagram of fig.
2. Set a signal generator with peak to peak amplitude of 1V and a frequency of 5 KHz.
3. Note the input and output waveform on the CRO.
4. Repeat above steps for different input waveforms.
5. Plot the input and output waveforms.

INTEGRATOR:

COMPONENTS REQUIREMENT FOR INTEGRATOR:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	Function Generator	1
3.	CRO	1
4.	IC741	1
5.	Resistors: 12KΩ 270KΩ 0. 1µF	 2 1 1
6.	Bread Board, Connecting Wires	1set

DESIGN :

For $V_{o(p-p)}$= 4V, $V_{i\,(p-p)}$ = 10V,
f_{in} = 500 Hz
C_1>> stray capacitance

Let C_1 = 0.1µf (standard value)

$$\Delta t = \frac{T}{2} = \frac{1}{2f}$$

$$= \frac{1}{2\,x\ 500\,Hz} = 1\text{ms}$$

Δv = 4V

$$I_1 = \frac{C_1 \Delta v}{\Delta t} = \frac{0.1\mu f x\ 4V}{1ms}$$

=400µA

$$R_1 = \frac{V_i}{I_1} = \frac{5V}{400\mu A}$$

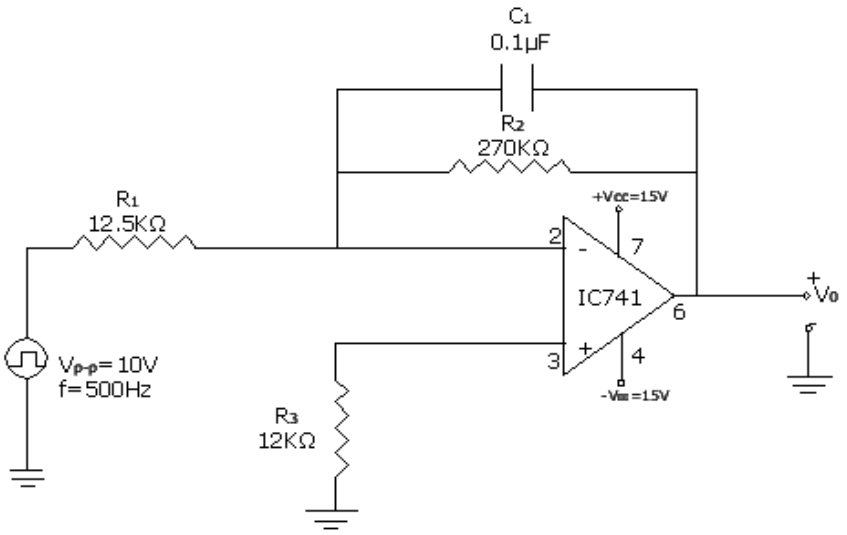
=12.5 KΩ

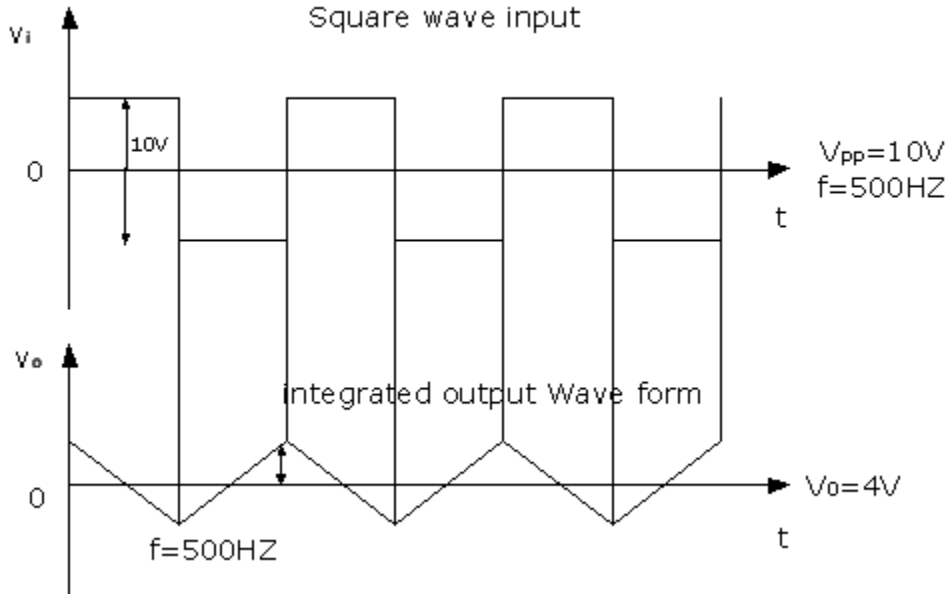
R_2= 20R_1= 20 X 12.5 KΩ

= 250KΩ (use a 270kΩ standard value)

R_3 = R_1=12.5KΩ(Use a 12kΩ standard value)

Integrator





PROCEDURE:

1. Connections are made as shown in the circuit diagram of fig.
2. Set the input signal as square wave from signal generator with peak amplitude of 5V and frequency 500Hz.
3. Note the input and output waveform on CRO.
4. Repeat the above steps for different input waveforms.
5. Plot the input and output waveforms.

RESULT:

	Input Frequency	Input voltage	Output voltage	Output frequency
Differentiator (Triangular)				
Integrator (Square)				

EXPERIMENT: 5

ASTABLE & MONOSTABLE MULTIVIBRATORS

AIM: To design and conduct an experiment using IC 555 timer
(a) Astable Multivibrator for given duty cycle.
(b) Monostable Multivibrator for a given pulse width.

a) ASTABLE MULTIVIBRATOR

COMPONENTS REQUIREMENT:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply 5V	1
2.	Function Generator	1
3.	CRO	1
4.	IC555	1
5.	Resistors: 3.3KΩ 2.2KΩ 4.7KΩ 1KΩ 1µF,0.01µF, 0.001 µF,0.1 µF 1N4007 Diode	 2 1 1 1 4 1
6.	Bread Board, Connecting Wires	1set

THEORY:

An Astable multivibrator is a circuit that is continuously switching its output voltage b/w high and low levels. It has no stable state. An Astable multivibrator using an operational amplifier is done when the circuit output is at the positive saturation level, current flows into the capacitor, charging it positive at the top. The output then rapidly switches to the op-amp negative saturation level. Now current flows from the capacitor removing its positive charge and recharging it with the opposite polarity. Then the recharging it with the opposite polarity. Then the op-amp output rapidly switches back to the positive saturation level and the cycle starts again.

It is seen that the circuit is a square wave generator with an O/P that swings b/w the op-amp positive and negative saturation levels.

(A) ASTABLEMULTIVIBRATOR

DESIGN:

$T_{HIGH}=0.69R_AC$

$T_{LOW} = 0.69R_BC$

Duty Cycle = $D=\frac{t_{HIGH}}{T}=\frac{R_A}{R_A+R_B}$

Frequency, $f=\frac{1}{T}$

i) Duty Cycle less than 50% (36%)

Frequency=200Hz. T=5ms

$$D=\frac{t_{HIGH}}{T}$$

Therefore $T_{HIGH} = T \times D$

$= 5\text{ ms} \times 0.36$

$T_{HIGH} = 1.8ms$

$T_{HIGH} = 0.69R_AC$

Let C =1µF

Therefore $R_A= 2.6k\Omega$ Use 2.2 KΩ(Std value)

$T_{LOW} = T- T_{HIGH} = 5ms-1.8ms=3.2ms$

$T_{LOW} = 0.69R_BC$

Therefore $R_B = 4.64k\Omega$ Use 4.7 KΩ std. value

ii) Duty Cycle more than 50% (64%)

Frequency = 200Hz

$$T=\frac{1}{f}=\frac{1}{200}=5msec.$$

D=0.64, let C=1µF

$D=\frac{t_{HIGH}}{T}$

$t_{HIGH}=DXT=0.64X5ms=3.2msec$

$t_{HIGH}=0.69XR_AC$

$R_A=\frac{t_{HIGH}}{0.69XC}=\frac{3.2msec}{0.69X110^{-6}}=4.6K\Omega$ (Select4.7KΩ)

$t_{Low}=T-t_{HIGH}=5m-3.2m=1.8msec.$

$t_{Low} = 0.69\ R_B C$

$R_B = \frac{1.8ms}{0.69X110^{-6}} = 2.6K\Omega$ (Select2.2KΩ)

iii) Duty cycle equal to 50%

Frequency = 200Hz

$T = \frac{1}{f} = \frac{1}{200} = 5msec.$

$D = \frac{t_{HIGH}}{T} = \frac{R_A}{R_A + R_B}$

$t_{HIGH} = 0.69R_A C \qquad t_{Low} = 0.69R_B C$

D=0.5

T=$t_{HIGH} + t_{Low}$

$t_{HIGH} = DXT$=0.5X5msec. = 2.5msec

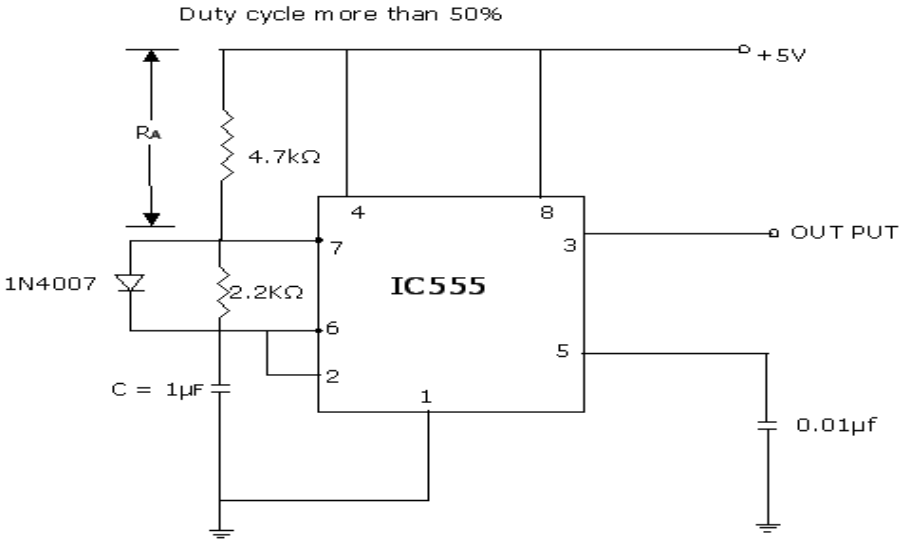
$t_{Low} = T - t_{HIGH} = 5m - 2.5m = 2.5msec.$

$t_{HIGH} = 0.69R_A C$

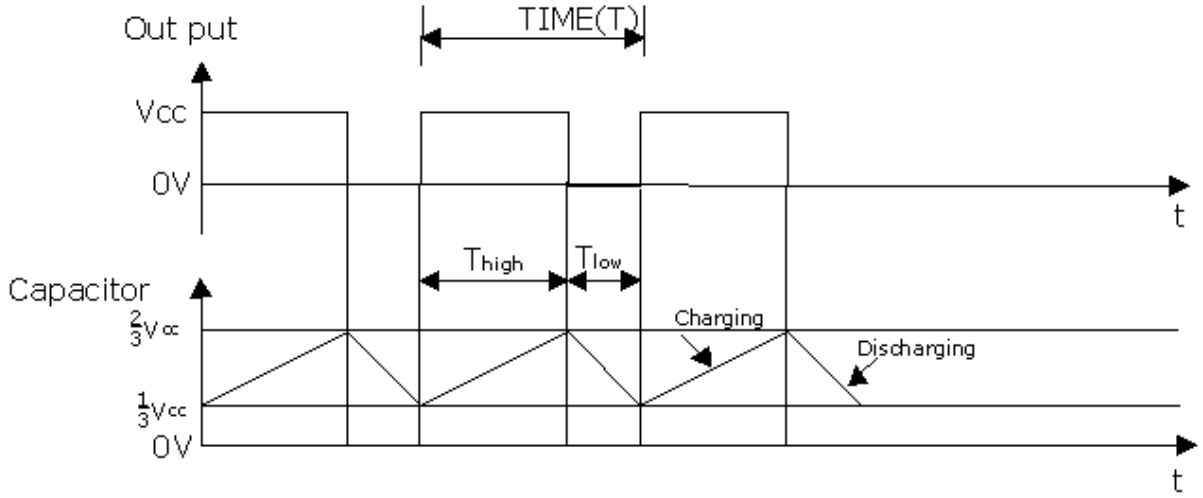
$R_A = \frac{t_{HIGH}}{0.69XC} = \frac{2.5msec}{0.69X110^{-6}} = 3.3K\Omega$

$R_A = R_B = 3.3K\Omega$

Astable Multivibrator



WAVE FORMS:
(Duty cycle > 50%



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Switch on the supply and note down the output waveform at pin no.3 onthe CRO.
3. Note T_{HIGH}=……
   T_{LOW}=……& V_{pp} =
4. Compare theoretical and practical time periods.
5. Draw the input and output waveforms for different duty cycles

Tabular Column for Astablemultivibrator

Duty cycle Theoretical	V_{pp}	T_{HIGH}	T_{LOW}	Duty cycle practical	**$Vc_{(P-P)}$**
36%					
50%					
64%					

(b) MONOSTABLEMULTIVIBRATOR

DESIGN:

Trigger input of frequency1Khz .i.e T=1m sec

Let t_p<T . Let t_p=0.1msec

t_p = 1.1RC

Let C = 0.1μF

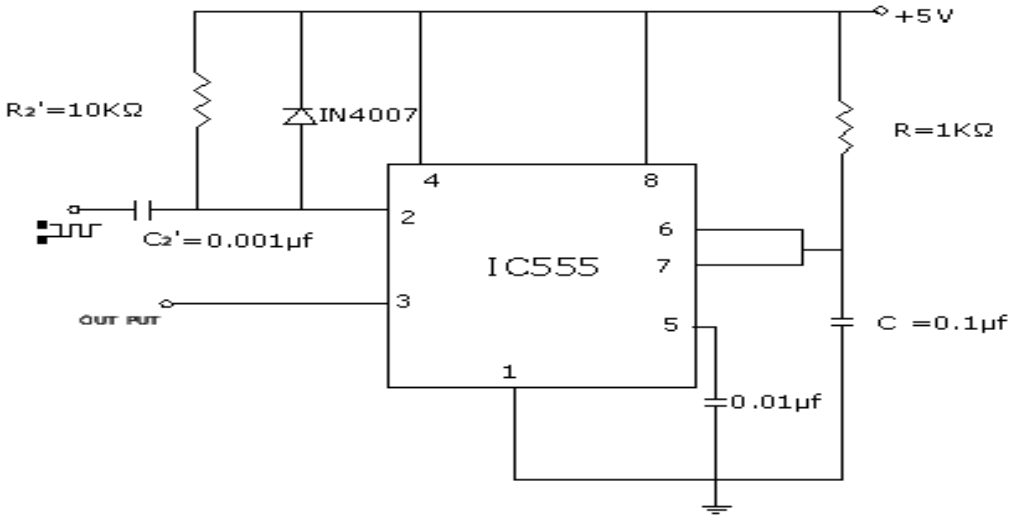
$$R = \frac{t_p}{1.1XC} = 1K\Omega$$

THEORY:

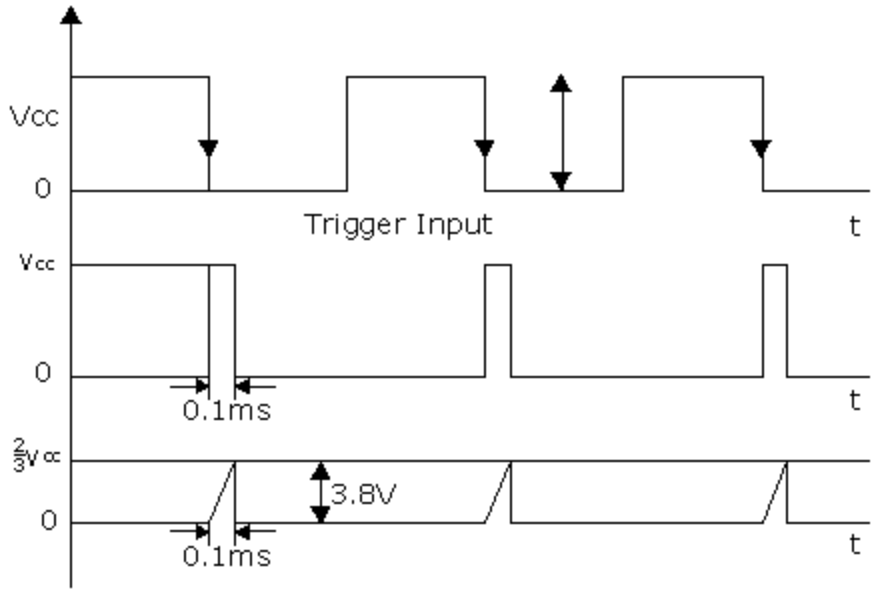
A Monostable Multivibrator has one stable output state. Its normal output voltage may be high or low, and it stays in the normal state until triggered. When triggered, the o/p switches to the opposite state for a time dependent on the circuit components.

The dc conditions of the circuit are that the op-amp inverting input terminal is grounded via resistor R_3 and the non inverting input terminal is biased positively by resistor R_1 and R2. Consequently the op-amp o/p is normally positive saturation level and the capacitor C2 is charged with the polarity. If C2 was not present, the circuit would be similar to capacitor-coupled voltage level detector that switches its o/p from $+V_o$ to $-V_{sat}$

Monostable Multivibrator



WAVE FORMS:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Switch on the supply (V_{CC}=5V)
3. Give a trigger input to pin No 2.
4. Note down the waveform at pin no.3.
5. Observation: t_p=

RESULT:

Theoretical Pulse width t_p = _____

Practical pulse width t_p = _____

EXPERIMENT: 6

GENERATION AND DETECTION OF PULSE SAMPLING (PAM) AND FLAT TOP SAMPLING

a) PULSE SAMPLING (PAM)

AIM: To demonstrate an experiment to generate a pulse sampled signal and its reconstruction.

COMPONENTS REQUIRED:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply 5V	1
2.	Function Generator	1
3.	CRO	1
4.	Transistor SL100	1
5.	Resistors: 10KΩ 22KΩ 4.7KΩ 10KΩ pot 0.1μF	 1 1 1 1 1
6	OA79 Diode	1
7.	Bread Board, Connecting Wires	1set

THEORY:

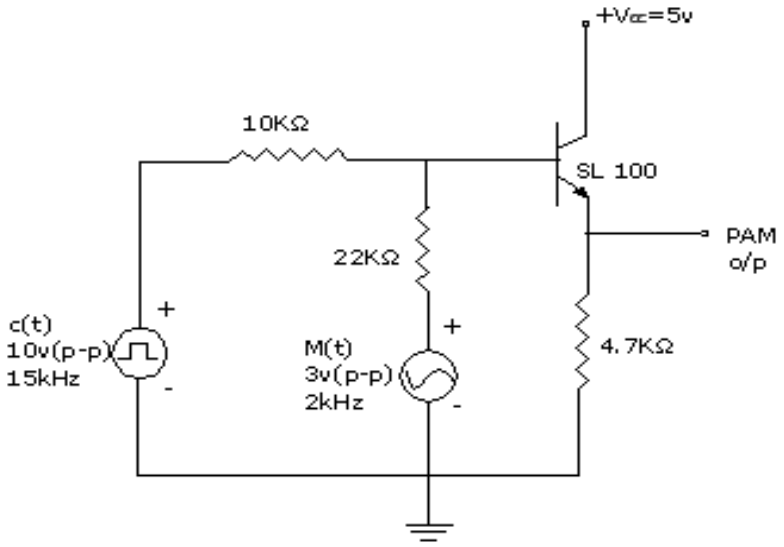
In pulse amplitude modulation (Pam) the amplitude of the pluses are varied in accordance with the modulating signal denoting the modulating signal as m (t) signal. The balanced mixer/modulators are frequency used as multipliers for this purpose. The O/P is a series of pluses, the amplitudes of which vary in proportion to the modulating signal.

The particular form of amplitude modulation is referred to as natural PAM because the tops of the pluses follow the shape of the modulating signal.

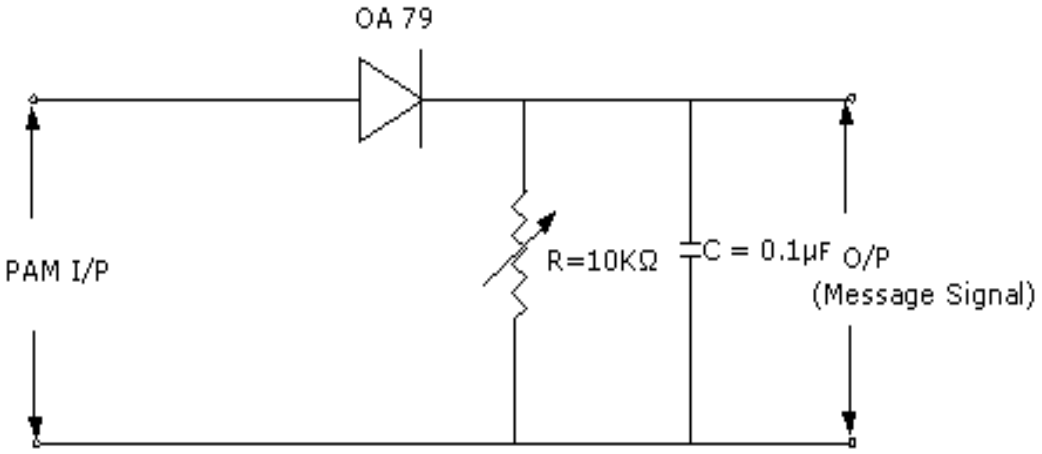
As shown in figure the samples are taken at regular interval of time. Each sample is a pulse, whose amplitude is determined by amplitude of the variable at the instant of time at which the sample is taken. If enough samples are taken, the receiving end. This is known as "Pulse amplitude modulation".

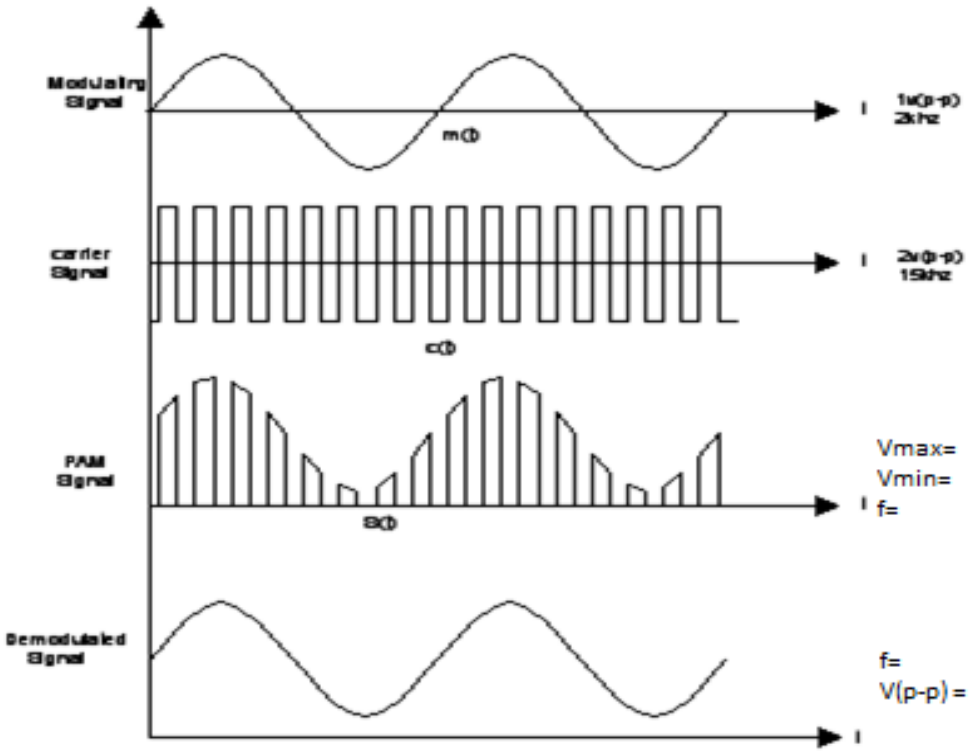
The sampling theorem sates that, if the sampling rate in any pulse modulation system exceeds twice the maximum signal frequency, the original signal frequency, the original signal can be reconstructed in the receiver with minimal distortion.

Pulse Amplitude Modulation(PAM)



Demodulation Circuit For PAM





Wave Forms

PROCEDURE:

1. Make the connections as shown in circuit diagram.
2. Set the carrier amplitude to around 10V (p-p) and frequency in the range of 5 kHz to 15 kHz.
3. Set the signal amplitude to around 3V (p-p) and frequency to 2 kHz.
4. Connect the CRO at the emitter of the transistor and observe the PAM waveform.
5. Now to verify sampling theorem, keep the modulating signal frequency to say 2 kHz and the carrier frequency to twice that of modulating signal frequency and observe the output waveform. Connect this output to the demodulator circuit and observe the signal if it matches with the signal then sampling theorem is verified.
6. Check the demodulated output for different frequencies of carrier wave.
7. Plot the waveforms.

Observations

Output voltage od Flat top sampled signal
Vmax=
Vmin=
Demodulated Signal
Vo=_____ at f= _____

b) FLATTOP SAMPLING

AIM: To demonstrate an experiment to generate a flat top sampled signal and its reconstruction.

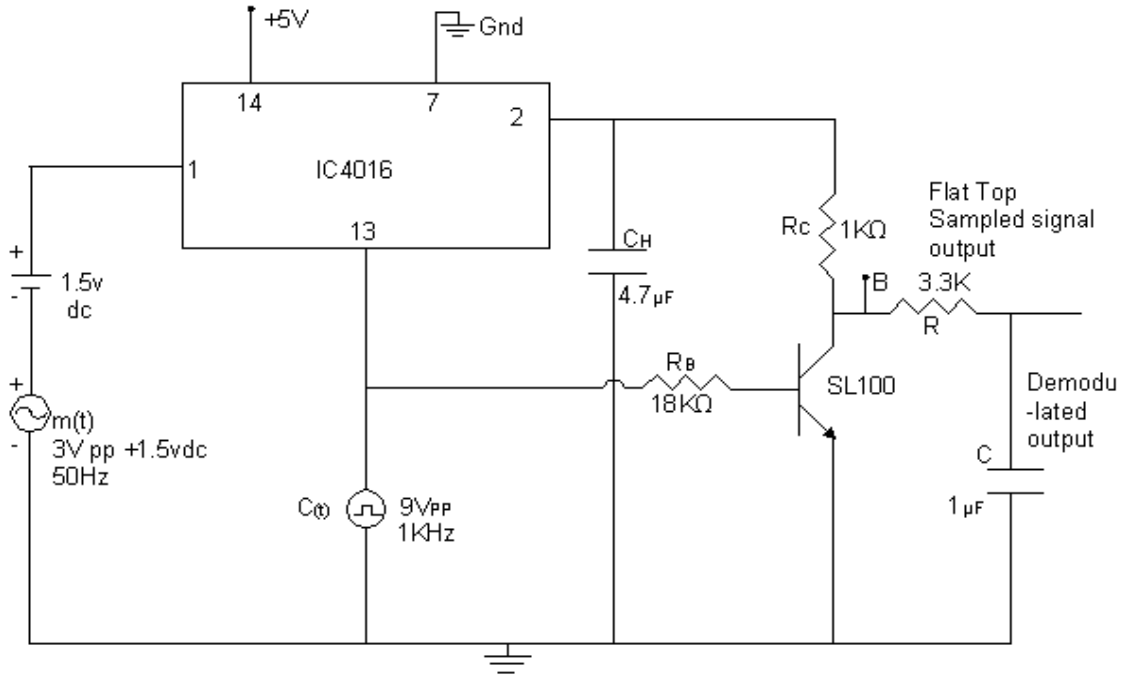
COMPONENTS REQUIREMENT:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply 5V	1
2.	Function Generator	1
3.	CRO	1
4.	IC4016	1
5.	SL100	1
6.	Resistors: 18KΩ 1KΩ 3.3KΩ 4.7 µF 1µF	 1 1 1 1 1
7.	Bread Board, Connecting Wires	1set

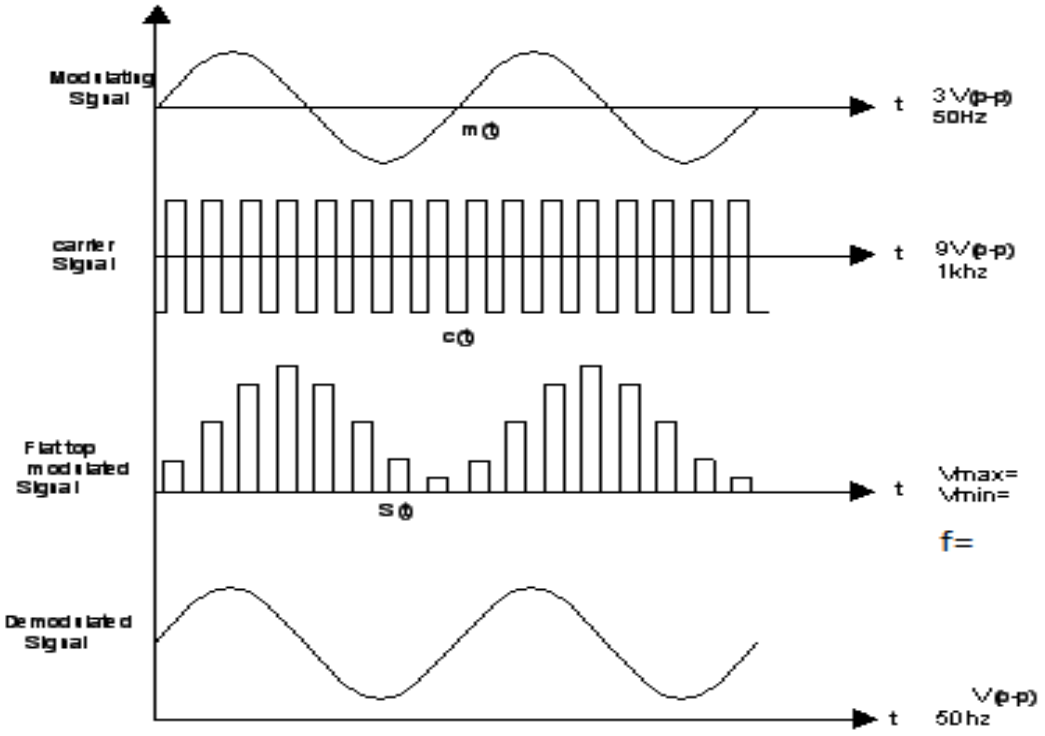
THEORY:

During transmission nose is introduced at the top of the transmission pulse which can be easily removed if the pulse is in the form of flat top here top of the samples are flat. That is they have constant amplitude. Flat top sampling makes use of sampled and hold circuit for the generation of flat top sampling can be mathematically considers as convolution of the sampled signal and the pulse signal. It is mostly used in digital transmission, the top of the slice does not preserve the shape of the waveform.

FLAT TOP SAMPLING



Flat Top Sampling Wave Forms



PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Set the sinusoidal modulating signal for amplitude of about 3V peak to peak at 50Hz signal and apply DC voltage of 1.5V to the input of the circuit simultaneously.
3. Square wave of carrier signal amplitude 9V peak to peak at 1KHz.
4. Check the output of flap top sampled signals at the collector of the transistor. Also check the demodulated output across the capacitor.
5. Calculate the amplitude (Vmax and Vmin) and frequency of modulated signal.
6. Calculate the amplitude and frequency of demodulated signal.

Observations

Output voltage Vo Flat top sampled signal
Vmax=
Vmin=
Demodulated Signal
Vo=_____ at f= _____

RESULT:

Flat top sampled signal is generated and demodulated.

EXPERIMENT: 7

GENERATION AND DETECTION OF AMPLITUDE MODULATION (COLLECTOR MODULATION)

AIM: To design and conduct an experiment for the generation and demodulation of AM.

COMPONENTS REQUIRED:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply 5V	1
2.	Function Generator	1
3.	CRO	1
4.	1:1 Transformer	1
5.	SL100	1
6.	IFT 455KHz	1
6.	Resistors: 100KΩ 10Ω 39KΩ 4.7 µF 0.01µF	 1 1 1 1 3
7.	Bread Board, Connecting Wires	1set

THEORY:

Figure shows the basic circuit for a BJT modulator. It is a high power class C amplifier with high-level modulators. The modulator is a linear power amplifier that takes the low modulating signal and amplifies it to a high power level. The modulating output signal is coupled through modulating transformer T_1 to the class C amplifier. The secondary winding of the modulation transformer is connected in series with the collector supply voltage V_{cc} of the class C amplifier. This means that modulating signal is applied in series with the collector power supply voltage of the class C amplifier applying collector modulation.

In absence of modulating input signal, there will be zero modulation voltage across the secondary of T1.Therefore, the collector supply voltage will be applied directly to the class C amplifier generating current pluses of equal amplitude and the output of the tuned circuit will be a steady sine wave.

When the modulating signal; occurs, the a.c voltage across the secondary of the modulating transformer will be added to and subtracted from the collector supply voltage. This varying supply voltage is then applied to the class C amplifier, resulting in variation in the amplitude of the carrier sine wave in accordance with the modulated signal. Due to this amplitude of the

current pluses also vary in accordance with the modulating signal. The tuned circuit then converts the current pluses in to an amplitude-modulated wave as shown in figure.

DESIGN:

Modulation Design

Given f_c= 500 KHz
$T = 1/f_c = 1/500X10^3 = 2\mu sec$

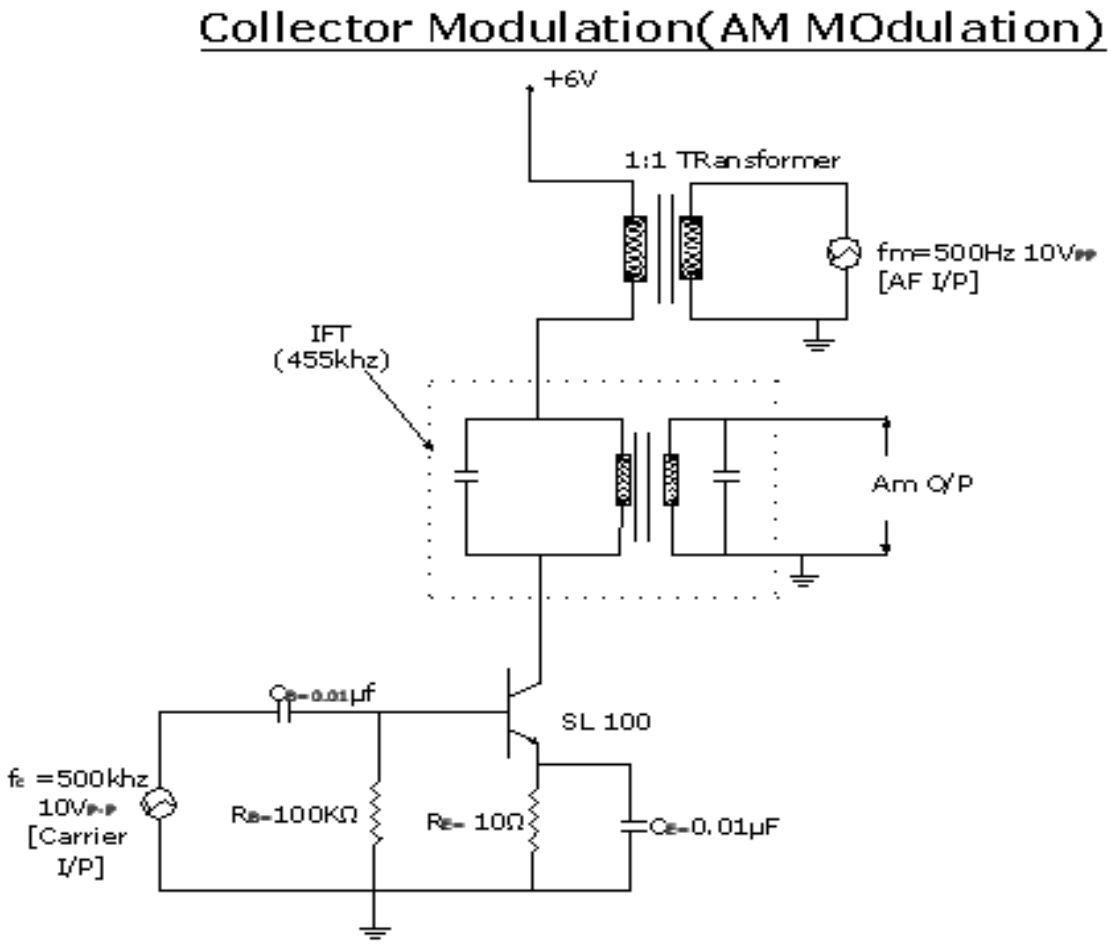
a) To design Base Clamping Circuit

$R_BC_B >> 20T$

That is $R_BC_B >> 40\mu sec$

Let R_B = 100k and C_B = 0.01μf

Therefore R_BC_B = 1000μsec>>40μsec



Demodulation Design

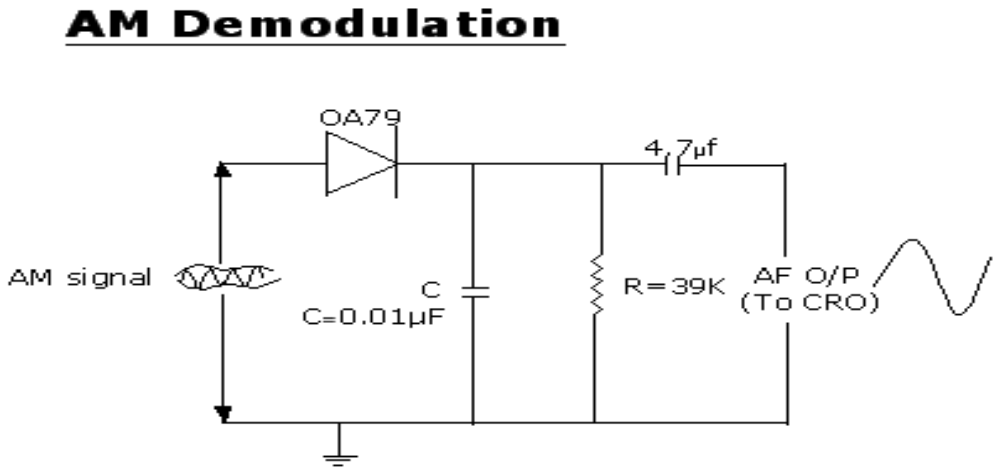
$1/f_m >> RC >> 1/f_c$

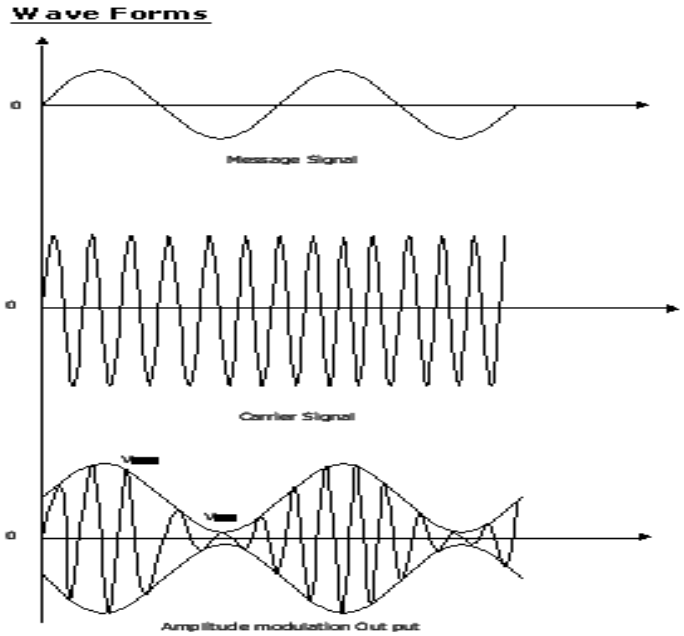
Let $RC >> 10/f_c$; f_c=455 KHz

f_m=500hz

Choose C=0.01μf

R=39k RC=390μsec>>10/fc





PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Switch off the AFT (Modulating Input) of modulating signal. For carrier frequency f_c of the modulating signal, adjust the carrier frequency to get max output.
3. Switch on the modulating signal and adjust amp about 5v p-p, frequency to 1-2 KHz& obtain an undistorted amplitude modulated output.

Observations

CarrierInput Voltage = 10V (Constant) AF I/P Voltage= 10V (Constant)

AF I/P	Carrier I/P	E_{max}	E_{min}	% m=(E_{max} –E_{min}) /(E_{max}+ E_{min}) x 100
$V_{i=}$ $f_{i=}$	$V_{c=}$ $f_{c=}$			

AM Demodulation

Output voltage Vo=_____ at f=_____

RESULT:

AM wave is generated and demodulated.

EXPERIMENT: 8

BJT MIXER UP/DOWN CONVERSION

AIM: To design a transistor mixer circuit using BJT and demonstrate the mixing action (up & Down Conversion) for an IFT of 455 KHz

COMPONENTS REQUIREMENT:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply 5V	1
2.	Function Generator	1
3.	CRO	1
4.	Transistor SL100	1
5.	IFT 455KHz	1
6.	Resistors: 47KΩ 470Ω 2.2KΩ 1KΩ 0.1μF	 1 1 1 1 2
7.	Bread Board, Connecting Wires	1set

THEORY:

Transistor mixer is also known as RF amplifier. RF amplifier provides initial gain & selectivity. Figure shows the RF amplifier circuits. It is a tuned circuit followed by an amplifier. The RF amplifier is usually a simple class A circuit. A typical bipolar circuit is shown in figure.

The values of resistors R_1 and R_2 in the bi-polar circuit are adjusted such that the amplifier works as class A amplifier. The RF (input (Antenna) is connected through coupling capacitor (C_1) to the base of the transistor. This makes the circuit very broad band, as the transistor will amplify virtually any signal picked up by the RF input (Antenna). However the collector is tuned with a parallel resonant circuit to provide the initial selectivity for the mixer input. And also local oscillator input is connected through coupling capacitor to the emitter of the transmitter.

DESIGN:

Let IC=2mA,V_{CE}=3v
β=100 & VR_E=2v for BF 194 /SL 100
$R_E=V_{RE}/I_E=V_{RE}/I_C=V_{RE}/I_C$=2v/2ma=1kΩ
Because $I_E=I_C$
R_E=1kΩ
$V_{CC}=I_CR_C+V_{CE}+V_{RE}$

Therefore $I_C R_C = V_{CC} - V_{CE} - V_{RE}$

$= 6-3-2 = 1$volt

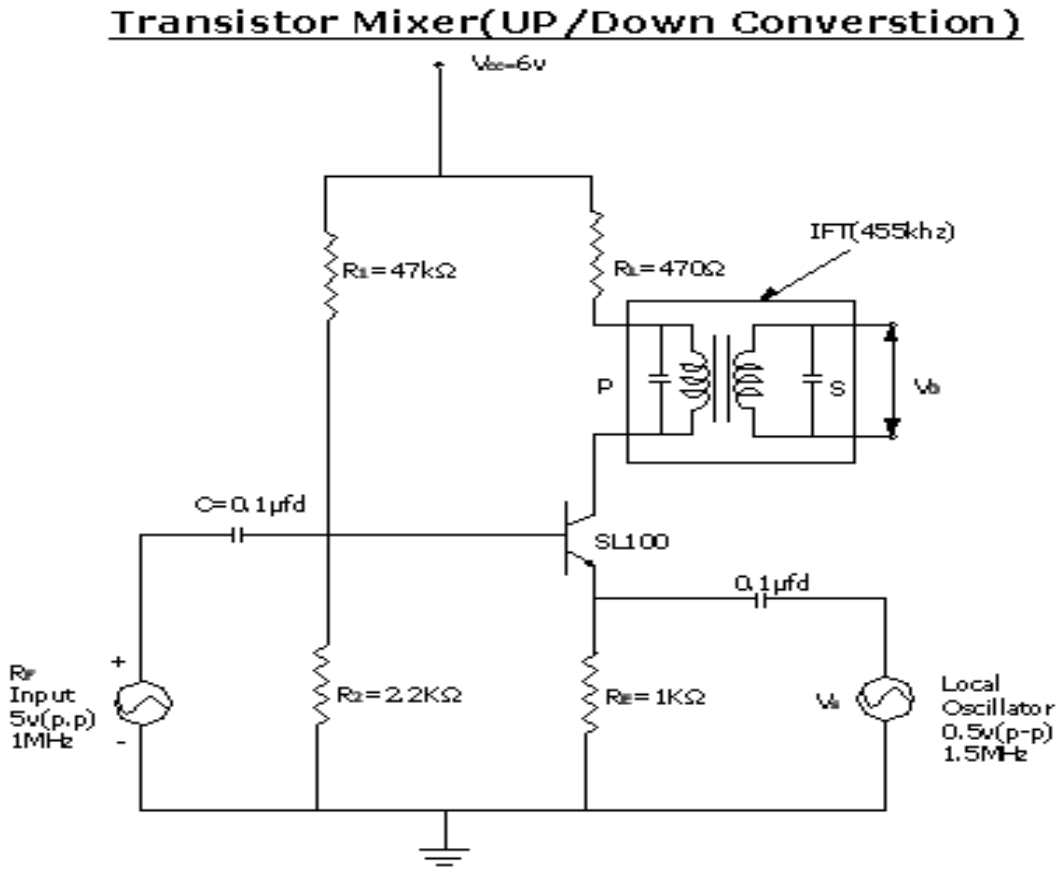
$R_C = 1/I_C = 1/2X109^{-3}$amps$= 500\Omega \approx 470\Omega$(Std.Value)

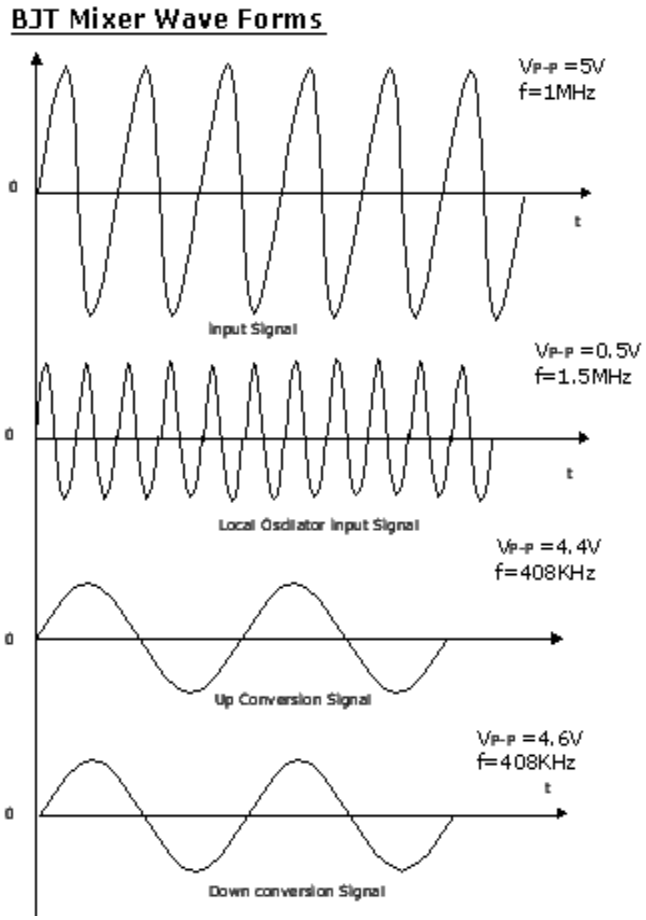
For Transistor to be in cut off Region

$R_2/R_1 = 1/20$ Therefore $R_1 = 20R_2$

Choose $R_2 = 2.2K\Omega$

Therefore $R_1 = 44k\Omega$ choose $R_1 = 47k\Omega$





PROCEDURE:

1. Before wiring the circuit check all the components using Multi-meter.
2. Connect the IFT in between signal source and CRO. Measure the tuned frequency that is f_{IFT}=455kHz
3. Rig up the circuit using the same IFT.
4. Switch ON the signal source V_1& V_2 (Use always MHz frequency range). Adjust V_2 amplitude to be 10 times larger than V_1.
5. For Ex: V_1=5v(p-p) & V_2=.0.5v (p-p)
6. Vary the frequency of RF source V_1 & local oscillator source V_2 such that we can see undistorted & sine wave on CRO>
7. Note down V_1& V_2 the difference should be equal to IFT frequency=455kHz
8. For up conversion $f_{osc}>f_{RF}$and for down conversion $f_{RF}>f_{osc}$.
9. Verify the same and tabulate readings in Tabular column.

RESULT:

f_s	f_0	Difference frequency
		Vo =____ at f = _____

EXPERIMENT: 9
INSTRUMENTATION AMPLIFIER

AIM: To design Instrumentation amplifier of differential mode gain A using three amplifiers.

COMPONENTS REQUIREMENT:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±15V	1
2.	Function Generator	2
3.	CRO	1
4.	IC741	3
5.	Resistors: 3.9kΩ 8.2 kΩ 220kΩ 1kΩ Pot	 2 2 2 1
6.	Bread Board, Connecting Wires	1set

THEORY:

The instrumentation amplifier circuit is a combination of the differential input /output amplifier (stage 1) and the difference amplifier (stage 2). The difference amplifier uses the differential output voltages from the differential input/output amplifier to drive a grounded load, as illustrated. For instrumentation purposes, most loads have one grounded terminal, otherwise ground loops and static electricity could cause problems. So, the ability to drive a grounded load necessary. The differential input/output stage offers a very high input resistance at each input terminal.

DESIGN:

To design an instrumentation amplifier for an overall voltage gain of 900 with an input of 15mVusing 741 op-amps with a supply voltage of ±15V.

Let $A_{V1} \approx A_{V2}$
$= \sqrt{A_V} = \sqrt{900}$
$= 30$
$I_2 >> I_{B(max)}$
$I_2 >> I_{B(max)} =$ 50µA

$R_2 = \frac{V_i}{I_2} = \frac{15mV}{50\mu A} = 300\Omega$ (Use 500 Ω variable)

$A_{V(diff)} = \frac{2R_1+R_2}{R_2}$

$R_1 = (A_{V(diff)}-1)R_2/2$

= 4.35K Ω(3.9KΩ Selected)

$R_3=R_1$ = 3.9K Ω

$V_0=A_VV_i$= 900 x 15 mv

= 13.5V

$I_{5(min)} >> I_{B(max)}$

I_5=100 $I_{B(max)}$ =50 μA

$R_5 = \frac{V_0}{I_5} = \frac{13.59}{50\mu A}$ = 270K Ω (standard value)

$R_4 = \frac{R_5}{A_{V2}} = \frac{270k\Omega}{30}$ = 9K Ω (Select 8.2K Ω standard value)

R_6 =R_4=9K Ω (Select 8.2K Ω standard value)

R_7= R_5± 20% ≈ 270K Ω ± 20%

≈ 216 k Ω to 324 k Ω(use 220 k Ω fixed resistor)

PROCEDURE:

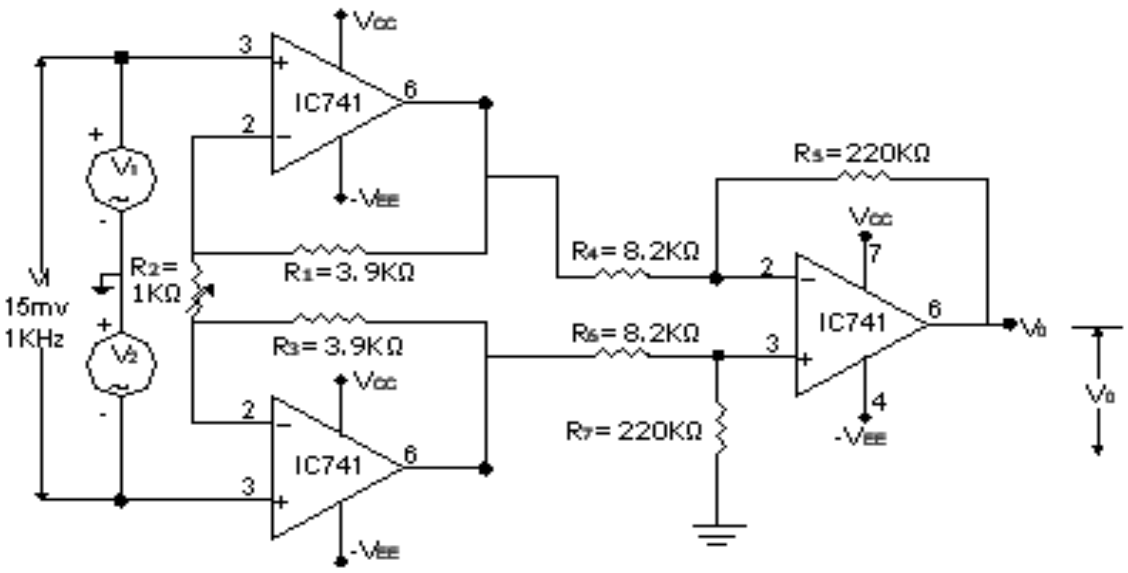
1. Connections are made as shown in the circuit diagram of fig1.
2. Apply ac input sine wave of peak amplitude of 15mV at a frequency of 1kHz from signal generators from the ckt. shown:
3. Check the power supply of +15V and -15V.
4. Vary the pot and observe the o/p till you get $V_0= A_v V_i$. Measure the o/p voltage and calculate A_V.

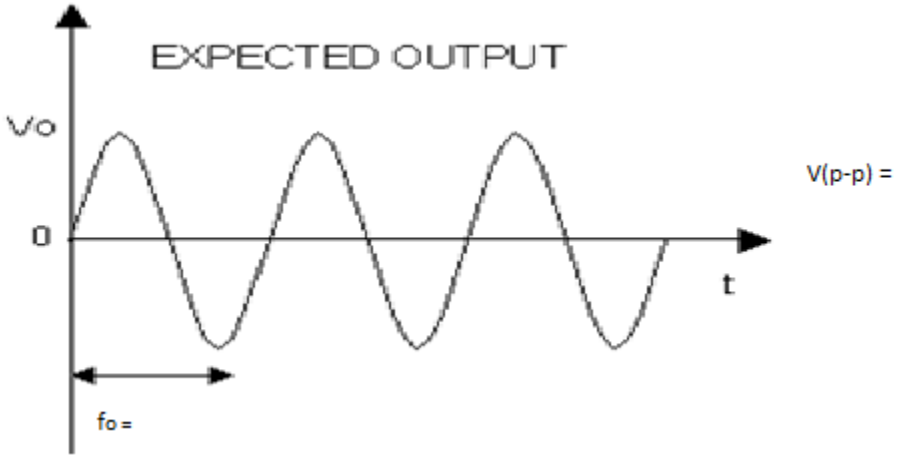
Observations:

Input voltage V_i= _____ at 1KHz
Output Voltage Vo=_____ at 1KHz
Gain A_v =_____

Instrumentation Amplifier

CIRCUIT DIAGRAM





RESULT:

Theoretical and Practical Gain of the instrumentation amplifier are verified.

EXPERIMENT: 10
FM MODULATION AND DEMODULATION

AIM: Demonstrate a suitable experiment to generate an FM signal using IC 8038 and its demodulation using IC565.

REQUIREMENTS:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±12V	1
2.	Regulated Power supply ±6V	1
3.	Signal Generator	1
4.	CRO	1
5.	IC 8038, IC565	2
6.	Capacitors : 0.01µF 0.001µF 10µF 1µF	 1 4 1 1
7.	Resistors: 12kΩ 82kΩ 100kΩ 10kΩ 1kΩ 47kΩ	 3 1 1 2 2 1

THEORY:

The IC 8038 waveforms generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangle, saw tooth and pulse waveforms with a minimum of external pulse components.

The frequency of the waveform generator is direct function of the dc voltage at terminal 8(measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (eg. +-10%)the modulating signal can be applied directly to pin8, merely providing dc de-coupling with a capacitor. An external resistor between pins 7 and 8 is not necessary but it can be used to increase input impedance from about 8k. (pins 7 and 8 connected together), to about (R+8kΩ).

The sine wave output has a relative high output impedance (1k typical). The circuit may use a simple op-amp follower to provide buffering, gain and amplitude adjustment.

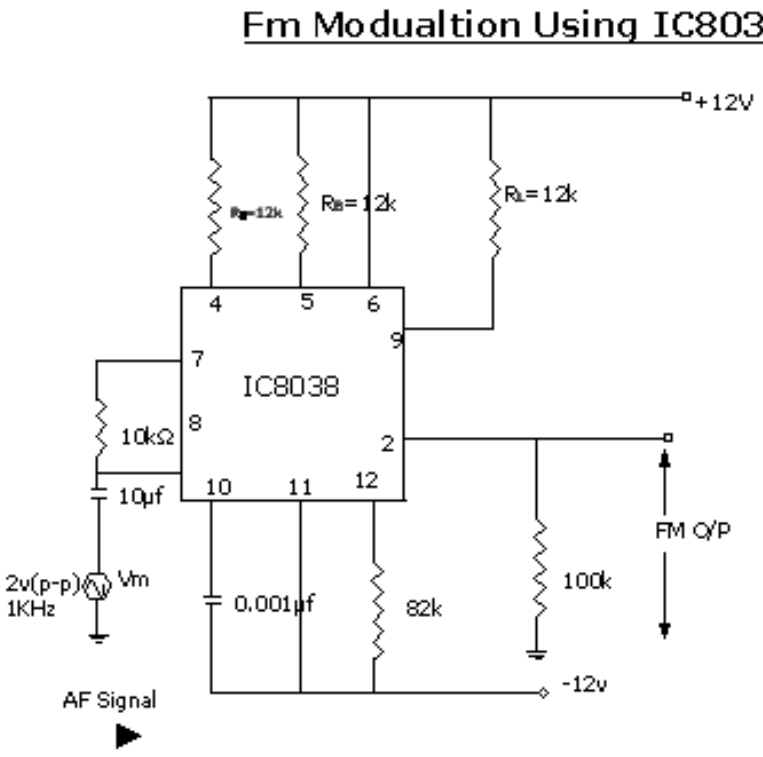
For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8.In this way the entire bias for the current sources is created by the modulating, and a very large (eg.1000: 1) sweep range is created (f=0 at V_{sweep}=0). Core

must be taken, however, to regulate the supply voltage, in this configuration the charge current and thus the frequency becomes dependent on the supply voltage. The potential on pin 8 may be swept down from V+by ($7/3V_{supply}$-2V).

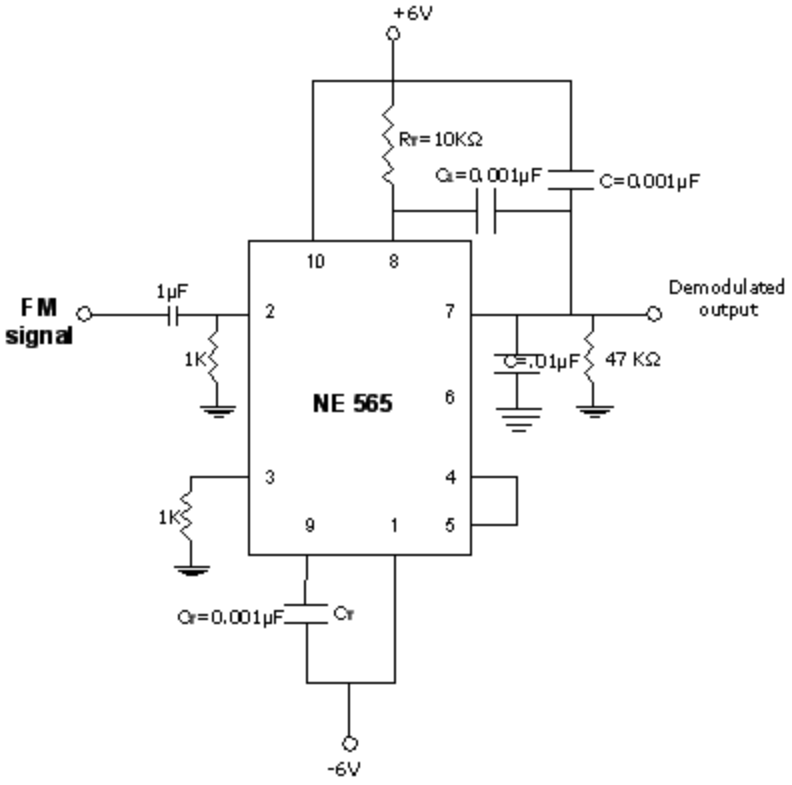
The IC 8038 is fabricated with advanced monolithic technology, using schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations.

Features

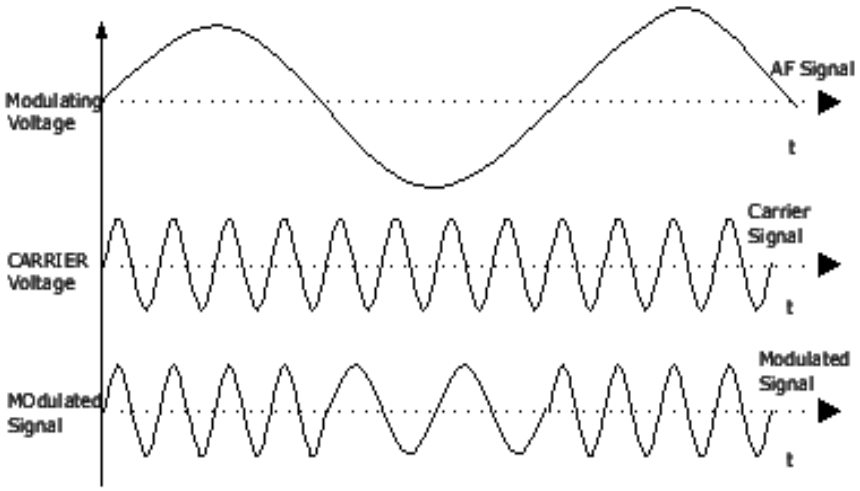
- Low-frequency drift with temperature.
- Simultaneous sine, square & triangular wave O/Ps
- Low distortion sine wave output.
- High linearity triangle wave output.
- Wide operating frequency range 0.001 Hz to 300 kHz.
- High-level output-TTL to 28V.
- Easy to use-just a handful of external components required.



Frequency Demodulation Circuit Diagram



Wave Forms



PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Apply +12V& -12V to the IC 8038 as supply voltage from regulated power supply.
3. For the modulation circuit observe the carrier waveform at pin number 2 by switching off the function generator. Note the carrier frequency.
4. Switch on function generator & apply a modulating signal of 2v peak to peak and frequency in the range of 1khz to 10khz through RC circuit as shown.
5. Observe FM output at pin 2 and measure f_1 and f_2.
6. Calculate frequency deviation Δf, modulation index β & transmission bandwidth B_T.
7. For FM demodulation, Connections are made as shown in circuit diagram.
8. Apply +6V & -6V to the IC565 as supply voltage from regulated power supply.
9. Apply FM Signal at pin 2. Connect one channel of CRO to pin 2 to display the signal.
10. Observe the demodulated signal at pin 7.
11. Measure the amplitude and frequency of demodulated signal.
12. Verify output signal frequency with respect to modulating signal applied to FM modulator.

Calculations:

Frequency deviation $\Delta f = f_2 - f_1$
Modulation index $\beta = \Delta f / f_m$
Transmission BW $B_T = 2(\Delta f + f_m)$

RESULT:

FM wave is generated using IC 8038 with

Modulation index β=……

Transmission BW B_T=……

Demodulated signal for FM is generated using IC565 with

Amplitude= ……

Frequency=……

EXPERIMENT: 11

FREQUENCY SYNTHESIS USING PLL

AIM: Conduct a suitable experiment to implement a frequency synthesizer circuit using IC 565 (PLL).

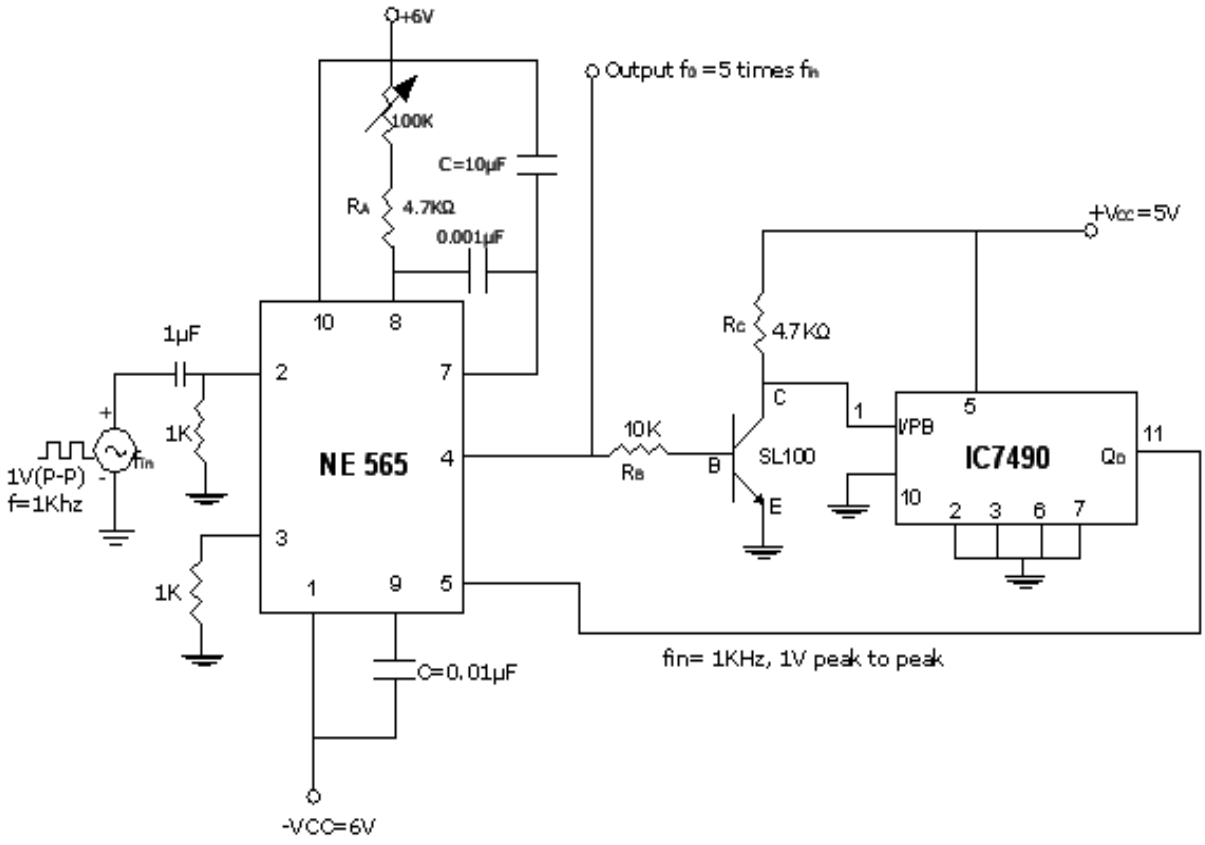
COMPONENTS REQUIRED:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply 5V	1
2.	Regulated Power supply ±6V	1
3.	Signal Generator	1
4.	CRO	1
5.	ICNE565	1
6.	Transistor SL100	1
7.	Capacitors :0.01µF, 0.001µF, 10µF, 1µF	Each 1
8.	Resistors: 100kΩ Pot 10kΩ 1kΩ 4.7kΩ	 1 1 2 2
9.	Bread Board, Connecting Wires	1

THEORY:

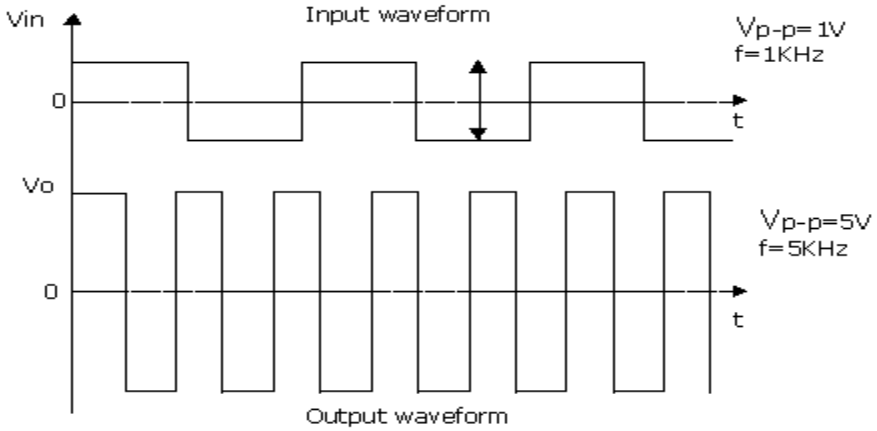
A frequency synthesizer is an electronic circuit that generates a range of frequencies from a single reference frequency. Frequency synthesizers are used in many modern devices such as radio receivers, televisions, mobile telephones, radiotelephones, walkie-talkies, CB radios, cable television converter boxes satellite receivers, and GPS systems. A frequency synthesizer may use the techniques of frequency multiplication, frequency division, direct digital synthesis, frequency mixing, and phase-locked loops to generate its frequencies. The stability and accuracy of the frequency synthesizer's output are related to the stability and accuracy of its reference frequency input. Consequently, synthesizers use stable and accurate reference frequencies, such as those provided by crystal oscillators.

A phase locked loop is a feedback control system. It compares the phases of two input signals and produces an error signal that is proportional to the difference between their phases.[10] The error signal is then low pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the phase error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the output is *locked* to the frequency at the other input. This other input is called the **reference** and is usually derived from a crystal oscillator, which is very stable in frequency. The block diagram below shows the basic elements and arrangement of a PLL based frequency synthesizer.



Frequency Sythesizer using PLL

Frequency Synthesis Waveforms:



PROCEDURE:

1. Make connections as shown in circuit diagram
2. Insert Mod -5 counters between pin 4 and 5 using SL 100 to IC 565 as shown.
3. Using function generators at pin 2 apply square wave signal of 1KHz frequency to get 1V p-p input signal.
4. By adjusting potentiometer 100K set the VCO frequency till PLL is locked, Measure and note down the output frequency at pin no 4. It should be 5 times the input frequency.
5. Measure the amplitude and frequency of the output signal.

RESULT:

Frequency synthesizer Output signal is generated for the given input signal with:

Amplitude = _____

Frequency = _____

EXPERIMENT: 12

BALANCED MODULATOR USING IC 1496

AIM: Using IC 1496 rig up a balanced modulator circuit test its operation and record the waveform.

COMPONENTS REQUIREMENT:

SL. NO.	COMPONENTS	QUANTITY
1.	Regulated Power supply ±12V	1
2.	Function Generator	1
3.	CRO	1
4.	IC1496	1
5.	Capacitors : 0.1μF	1
6.	Resistors: 47Ω 3.9kΩ 6.8 kΩ 10kΩ 1kΩ 47kΩ Pot	 4 2 1 2 3 1
7.	Bread Board, Connecting Wires	1set

THEORY:

The integrated circuit (IC) balanced mixer is widely used in receiver ICs, as well as being available as a separate integrated circuit. The IC versions are usually described as balanced modulation since the modulation function is basically the same as the mixing function. Integrated circuit doubly balanced modulation like the LM1496 operates as multiplier circuits that produce only side band pairs at the o/p. Application is simple, required only bias and an approximate band filter to eliminate side band pairs at harmonics of the carrier very little adjustment is required to obtain good balance.

An important advantage of the integrated circuit balanced modulator is that, when it is operated with a large carrier signal, the o/p signal amplitude is independent of the carrier amplitude. The result is the o/p amplitude depends only on the amplitude f the input signal (Which is the modulating signal when it is used as a modulator or the side band signal when it is used as a demodulator).

GENERAL DESCRIPTION:

LM1596/LM1496 Balanced Modulator-Demodulator:

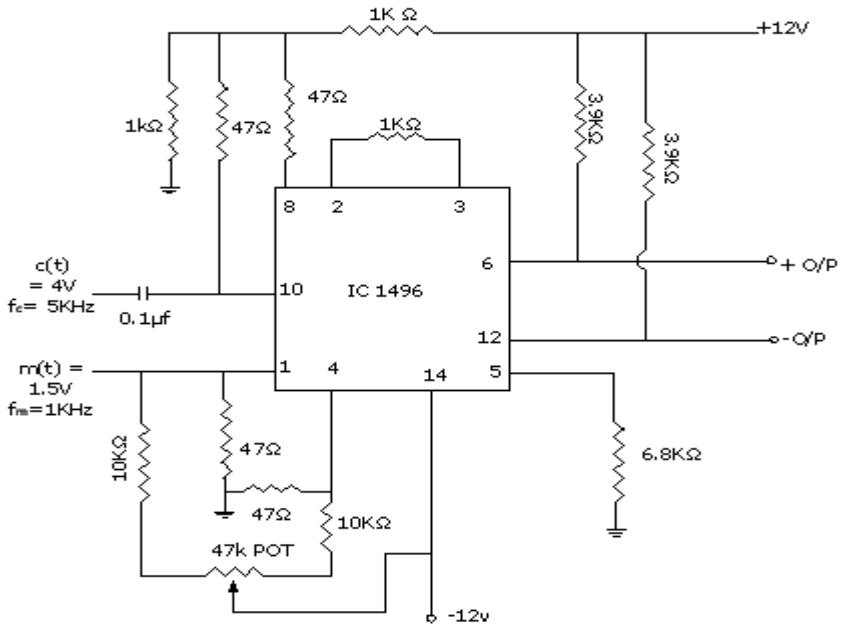
The LM1596/LM1496 are double balanced modulators-Demodulators which produce an output voltage proportional to the product of an input(signal)voltage and a switching(carrier)signal. Typical applications include suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection board band frequency doubling and chopping LM 1496 is specified for operation over the 0^0C to +70^0C temperature range.

FEATURES:

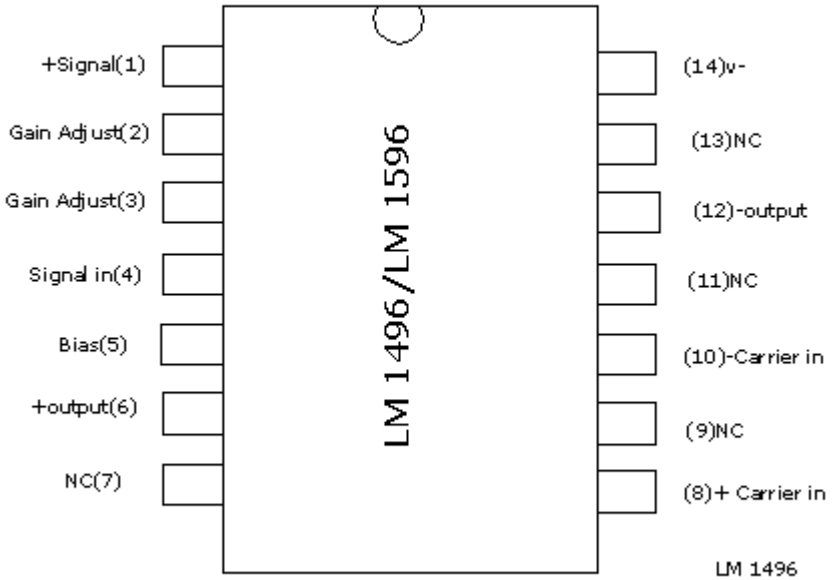
- Excellent carrier suppression
  65 dB typical at 0.5MHZ
  50 dB typical at 10 MHZ
- Adjustable gain and signal handling.
- Fully balanced input & output.
- Low offset and drift.
- Wide frequency response up to 100 MHZ.

The equivalent internal circuitry and 14-pin Dip pin out for the LM1496 are shown in fig. (b) &(c)
The circuit consists of two differential pairs with cross-coupled open collectors a biasing current source, and a modulation input section signals that are applied to the carrier & modulation inputs are multiplied together, and the product is scaled by the gain of the circuit. The LM1496 id designed to operate with carrier frequencies up to 100 MHz
Balanced modulator is commonly used in radio transmitter and receiver circuitry.

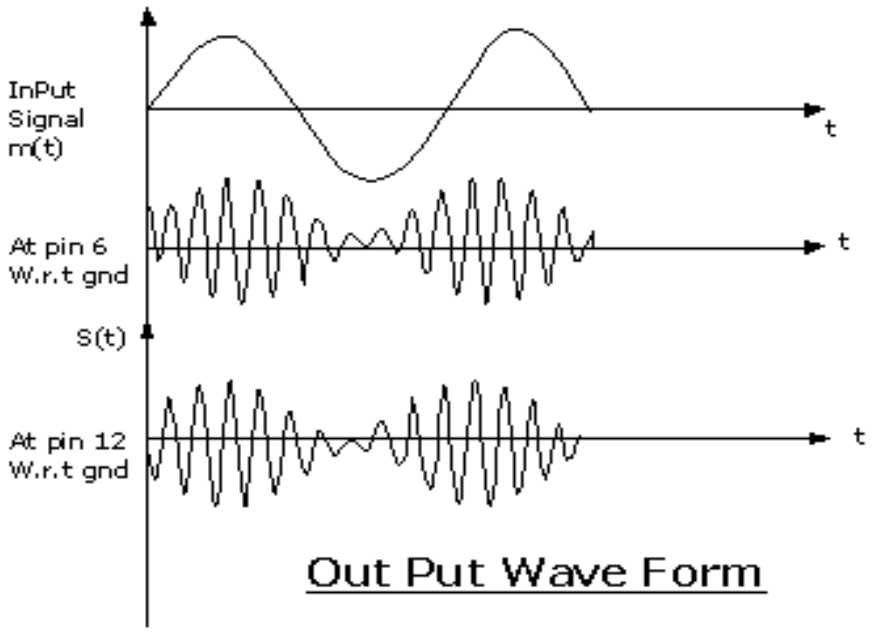
Balanced Modulator Using IC 1496



Pin Details



LM 1496
Top View
Fig(b)



Out Put Wave Form

PROCEDURE:

1. Make the connections as shown in circuit diagram.
2. Apply +12V & -12V to the IC 8038 as supply voltage from regulated power supply.
3. Set the carrier wave amplitude and frequencies and also the modulating signal amplitude and frequencies so as to get the DSBSC wave.
4. Check for the positive and negative o/p voltage at pin no.6 & 12 With respect to ground.
5. Observe the phase reversals at the cross point.

RESULT:

DSBSC signal is generated using Balanced Modulator IC1496.

K S INSTITUTE OF TECHNOLOGY, BENGALURU

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

RUBRICS for Evaluation in Laboratories

Record	Evaluation criteria		
	Good	**Average**	**Poor**
10 marks	The Record meets all aspects of assessment-Timeliness, contents, correctness, completeness & neatness.	The Record partially meets all aspects of assessment-Timeliness, contents, correctness, completeness & neatness.	The Record written poorly, does not meet all aspects of assessment-Timeliness, contents, correctness, completeness & neatness.
	9 to 10 marks	**5 to 8 marks**	**0 to 4 marks**
Observation & Conduction	**Evaluation criteria**		
	Good	**Average**	**Poor**
10 marks	The Observation meets all aspects of assessment-Timeliness, contents, correctness, completeness & neatness. Conduction of experiment is satisfactory.	The Observation partially meets all aspects of assessment-Timeliness, contents, correctness, completeness & neatness. Conduction of experiment is partially satisfactory.	The Observation poorly written and does not meet all aspects of assessment-Timeliness, contents, correctness, completeness & neatness. Conduction of experiment is not satisfactory.
	9 to 10 marks	**5 to 8 marks**	**0 to 4 marks**
Viva	**Evaluation criteria**		
5 marks	All questions answered Correctly	Answers are partially correct	Poorly answered
	5 marks	**3 to 4 marks**	**0 to 2 marks**
CIE - 15 Marks			
Write-up: 15% of maximum marks		**Conduction**: 70% of maximum marks	**Viva**: 15% of maximum marks
Total Marks : 40			
Record, Observation &Viva : 25 Marks			**CIE : 15 Marks**

HEAD OF THE DEPARTMENT
Dept. of Electronics & Communication Engg
K.S. Institute of Technology
Bengaluru - 560 109