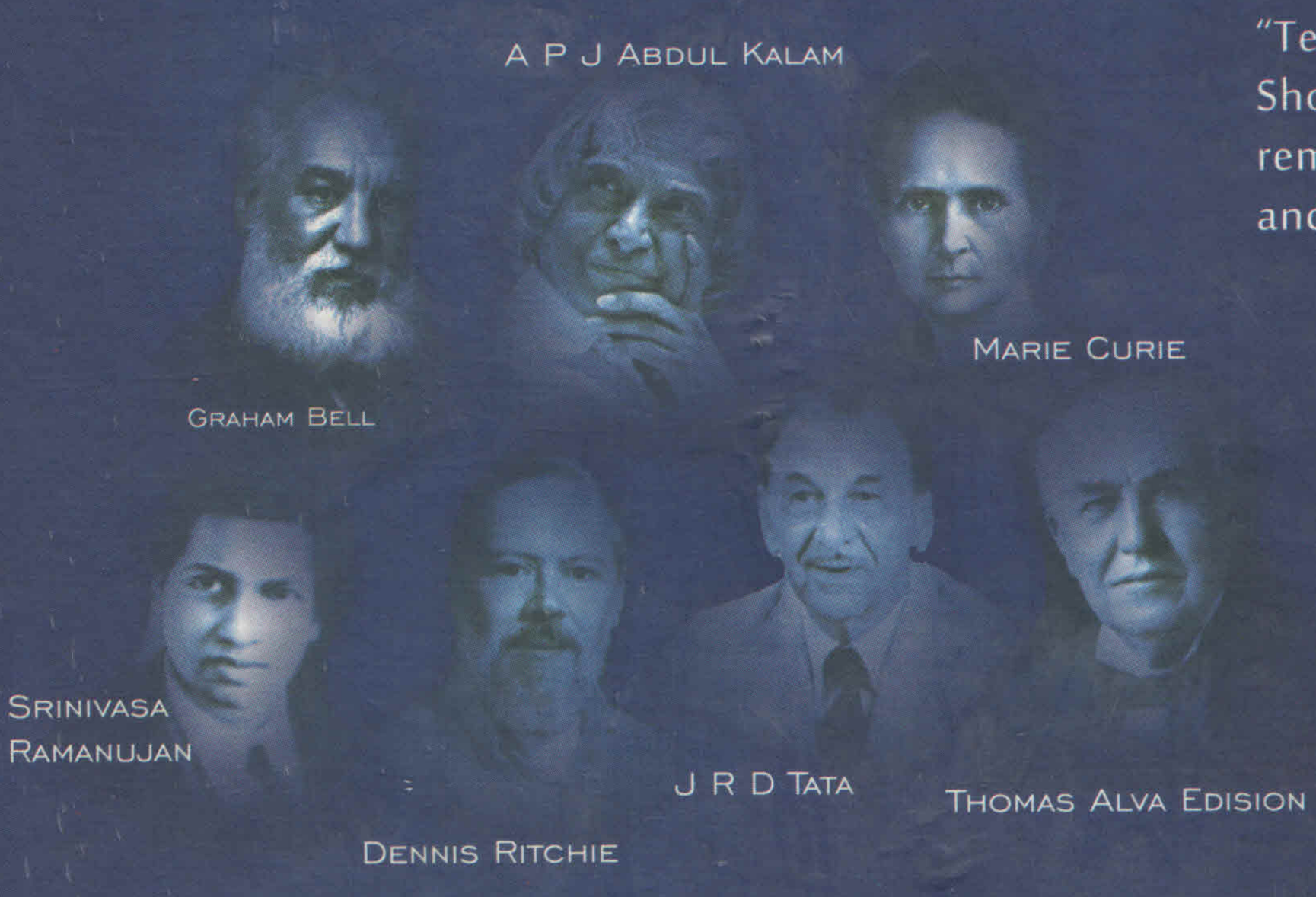
Kammavari Sangham (R)-1952

K.S.GROUP OF INSTITUTIONS

K.S. INSTITUTE OF TECHNOLOGY

(Approved by AICTE & Affiliated to VTU)

KANAKAPURA ROAD, BANGALORE - 560 109



"Tell me and I'll forget;
Show me and I may
remember; Involve me
and I'll understand"

PRACTICAL RECORD

NAME : DEVIYANI. G

SEM/ BRANCH : IV th SEM / ECE

SUBJECT & CODE : LIC LAB

USN : 1 K S 1 7 E C 0 3 2

K.S. INSTITUTE OF TECHNOLOGY

VISION

"To impart quality technical education with ethical values, employable skills and research to achieve excellence"

MISSION

* To attract and retain highly qualified, experienced & committed faculty.
* To create relevant infrastructure
* Network with industry & premier institutions to encourage emergence of new ideas by providing research & development facilities to strive for academic excellence
* To inculcate the professional & ethical values among young students with employable skills & knowledge acquired to transform the society

Kammavari Sangham (R)-1952

K.S.GROUP OF INSTITUTIONS

K.S. INSTITUTE OF TECHNOLOGY

ACCREDITED BY NAAC

(Approved by AICTE & Affiliated to VTU)

KANAKPURA ROAD, BENGALURU - 560 109

Laboratory Certificate

This is to certify that Mr./Ms. .....Deviyani.G.....
has satisfactorily completed the course of experiments in
Linear IC's & communication..laboratory, Code.....17ECL48
prescribed by Visvesvaraya Technological University, Belgaum for
the.....IV.....Semester B.E.....ECE.....Branch
in this College during the academic year 20..18..-20..19...

Name of the Candidate :.....Deviyani.G.....

USN :.....1KS17EC032.....Subject (with code).....Linear IC's & communication Lab 17ECL48

Internal assessment marks awarded :

22	12	34
25	15	40

Signature of Staff Incharge

Date: 15/05/2019

Signature of Head of Department

INSTRUCTIONS FOR MAINTAINING THE PRACTICAL RECORD

1. Record should be written neatly in ink on the right side page only, left side pages being reserved for diagrams and graphs in pencil.

2. Record should contain
   - Number and name of the Experiment
   - The date
   - Principle
   - Procedure
   - Observation calculation (to be entered on the left hand side pages in neat tabular forms wherever applicable)
   - Results

CONTENTS AND EVALUATION

Sl.No.	Date of Conducting Experiment	Date of Submission	Page No.	Title of the Experiment	Assessment Marks			Signature of Staff with Date
					Experiment 10 Marks	Record 5 Marks	Total	
1	13/02/19	20/02/19	1	Active low-Pass And High-Pass Filters (II Order)	9	10/4	23	20/2/19
2	20/2/19	27/2/19	6	RC Phase shift Oscillator & wein bridge Oscillator	10	10 3	23	Saluja 27/2/19
3	20/2/19	27/2/19	10	Adder, differentiator & Integrator.	10	9 4	23	
4	27/2/19	6/3/19	16	Digital to Analog Converter	10	10 4	24	Saluja 6/3/19
5	6/3/19	20/3/19	21	BJT Mixer UP/DOWN Conversion	10	10 3	23	Saluja 20/3/19
6.	20/3/19	3/4/19	25	Generation & detection of Pulse sampling (PAM) & flat-top Sampling	9	9 3	22	3/4/19
7	3/4/19	10/4/19	31	Astable & Monostable multivibrator.	10	9/3	22	10/4/19
8.	24/4/19	8/5/19	36	Collector amplitude Modulation	10	10/3	23	Saluja 8/5/19
9.	8/5/19	10/5/19	39	Instrumentation Amplifier	8	8/3	19	10/5
10.	8/5/19	10/5/19	41	FM Modulation & Demodulation	8	8/3	19	10/5
11.	10/5/19	15/5/19	46	Frequency synthesis Using PLL	8	8/3	19	15/5
12.	10/5/19	15/5/19	49	Balanced modulator usin IC1496	8	8/3	19	15/5
							20.5	

CONTENTS AND EVALUATION

Sl.No.	Date of Conducting Experiment	Date of Submission	Page No.	Title of the Experiment	Assessment Marks			Signature of Staff with Date
					Experiment 10 Marks	Record 5 Marks	Total	

22/25

DATE 13/02/19
EXP. NO. 1

EXPT TITLE: Active low-Pass and High-pass Filter (2nd order)

PAGE NO. 1

Aim :-

To design and conduct an experiment on active second order butterworth low pass filter and high pass filter for a given cut-off frequency and to plot the frequency response.

Components Required

SI NO.	Components	Quantity
1	Regulated Power supply ±15V	1
2	Function Generator	1
3	CRO	1
4	IC741	1
5	Resistors :	
	68kΩ	2
	150 kΩ.	1
	3300 pF	1
	1600 pF	1
6	Bread board, Connecting Wires	1set

Theory :-

A filter is a circuit that is designed to pass a specified band of Frequencies while attenuating all signals outside this band. Filter network may be either active or passive.
Passive filter networks contain only resistors, Inductors and capacitors.

Design :-

Second order Butterworth low pass filter for a given cut-off frequency of 1kHz.

$$R_1 + R_2 = \frac{70\,mV}{I_{B(max)}} = \frac{70\,mV}{500\,nA} = 140\,k\Omega.$$

$R_1 = R_2 = 70\,k\Omega$ (use 68 kΩ standard value)

$R_3 = R_1 + R_2 = 136\,k\Omega$ (use 150 kΩ standard value)

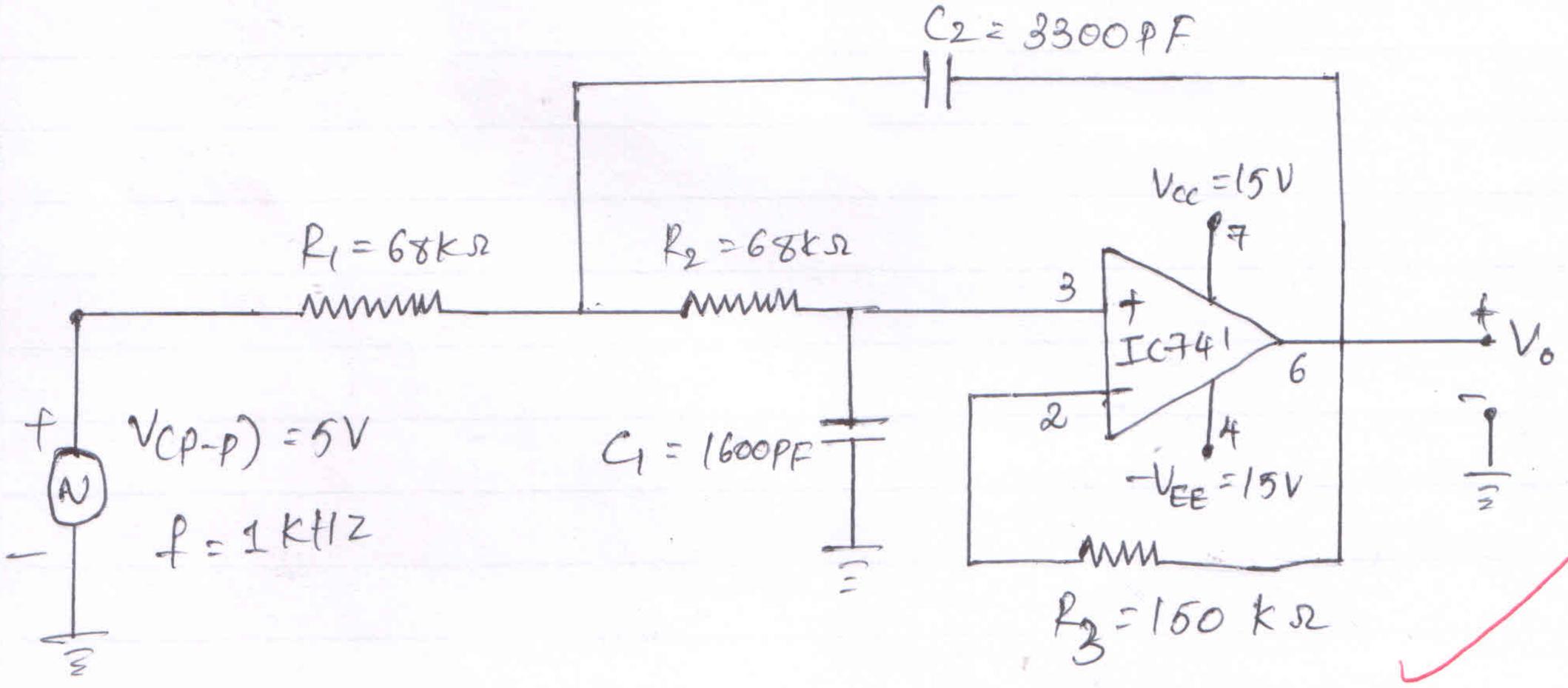
$X_{C_1} = \sqrt{2}\,R_2$ at f_c.

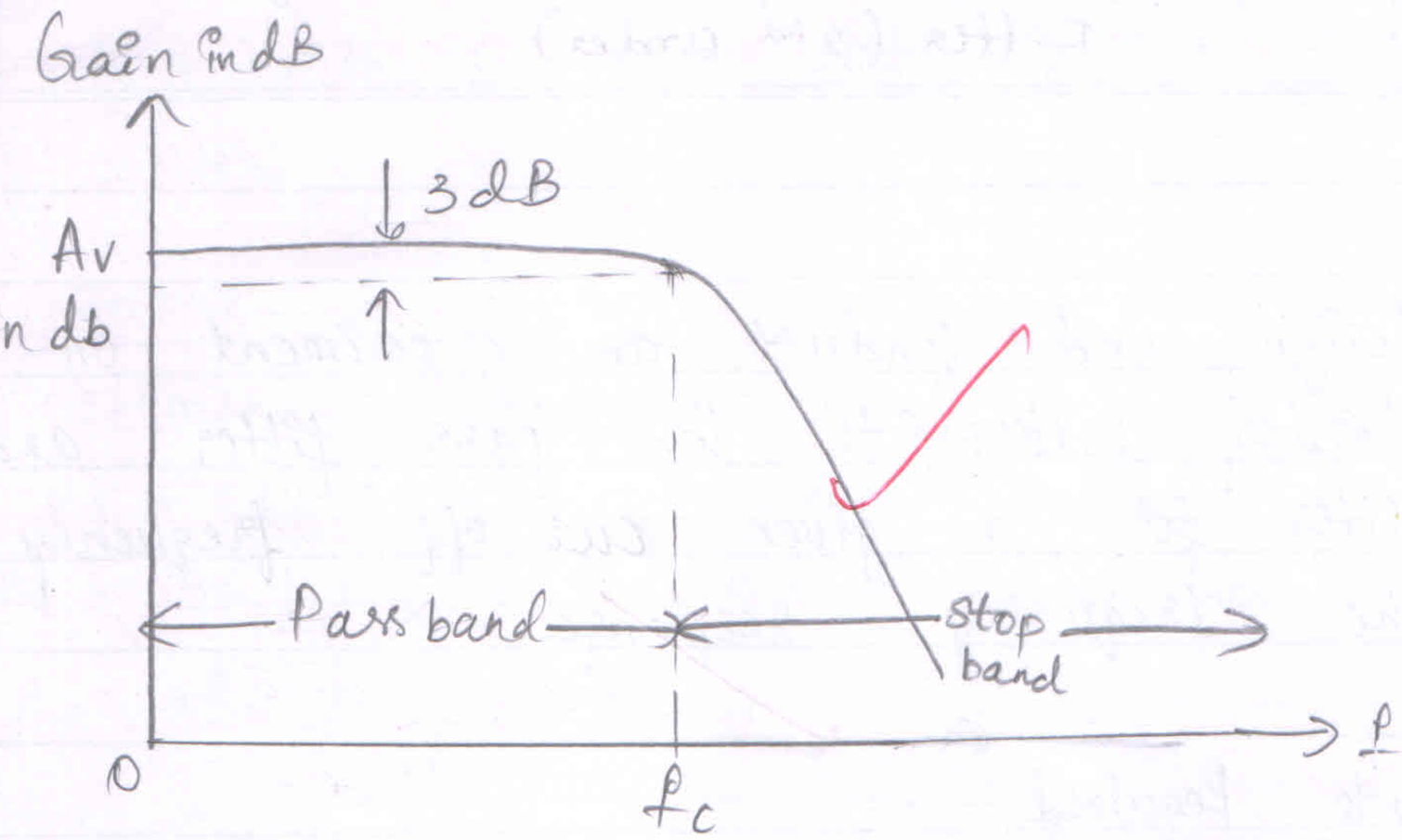
$$C_1 = \frac{1}{2\pi f_c \sqrt{2} R_2} = \frac{1}{2\pi \times 1kHz \times \sqrt{2} \times 68\,k\Omega}$$

$C_1 = 1655\,pF$ (use 1600 pF standard value)

$C_2 = 2C_1 = 2 \times 1000\,pF = 3200pF$ (use 3300pF standard value)

Second Order Low Pass Filter.





Expected Curve.

Tabulation.

Input Voltage $V_i = 5V$ Constant

Frequency Hz	o/p Voltage V_o	Gain = V_o/V_i	Gain in dB = $20\log_{10}(V_o/V_i)$
100	5	1	0
200	5	1	0
300	5	1	0
400	5	1	0
500	5	1	0
600	4.9	0.98	-0.175
700	4.6	0.92	-0.724
800	4.3	0.88	-1.110
900	4.4	0.84	-1.514
1000	3.6	0.72	-2.853
2k	1.20	0.24	-12.395
3k	0.520	0.104	-19.659
4k	0.320	0.064	-23.876
5k	0.240	0.048	-26.375
10k	0.080	0.016	-35.917

Active filter networks contain transistors or op-amps plus resistors & capacitors.

There are four types of filters.

- Low pass filters.
- High pass filters.
- Band pass filters.
- Band stop filters.

Low Pass Filter.

A low-pass filter is a circuit that has a constant output voltage from dc upto a cutoff frequency fc. As the frequency increases above fc, the output voltage is attenuated (decreases).

Figure shows a first order low-pass butterworth filter that uses an RC network for filtering. And the op-amp is used in the non-inverting configuration, hence it does not load down the RC network. Resistors R_1 & R_F determine the gain of the filter. The low-pass filter has a constant gain A_F from 0Hz to the high cutoff frequency fc. At fc the gain is 0.707 A_F and after fc it decreases at a constant rate with an increase in frequency. That is, when the frequency is increased tenfold (one decade), the voltage gain is divide by 10. In other words, the gain decreases 20dB (= 20 log(10) each time the frequency is increased by 10. Hence the rate at which the gain rolls off after fc is 20dB/decade by 10. where Octave signifies a two fold increase in frequency. The frequency $f = f_c$

Observation.

V_o = 3.6 V at f_c = 1 KHz

low pass filter	Cut off frequency (theoretical) f_c = 1 kHz	Cut off frequency (practical) f_c = 1kH

x10 x100 x1k x10k x100k

Second Order Active Low Pass Filter

0
-5
-10
-15
-20
-25
-30
-35
-40

$f_c = 1$ kHz.



Frequency

is called the cut off frequency because the gain of the filter at this frequency is done by 3dB (= 20 log 0.707) from 0 Hz, other equivalent terms for cut off frequency are 3-dB frequency, break frequency, or corner frequency.

Procedure :-

Rig up the circuit as shown in circuit diagram

Initially keep the Input voltage $V_m = 5V$ Constant at a frequency of 1kHz and observe the waveform.

keeping the input voltage constant at 5V, vary the frequency of the signal generator in steps of 100Hz and note down the corresponding output voltage on CRO.

Plot the graph using semi log sheet taking frequencies along X-axis and gain in dB along Y-axis.

Find the practical value of f_c from the graph

Compare theoretical and practical values.

Result :-

The maximum o/p voltage is 5

Thus, characteristics of low pass filter is verified.

Design.

Second order Butterworth high pass filter for a given cut-off frequency of 1.5 kHz.

$I_{B(max)} = 500\ nA$.

$$R_2 = \frac{70\ mV}{500\ nA} = 140\ k\Omega \text{ (use } 150\ k\Omega \text{ standard value)}$$

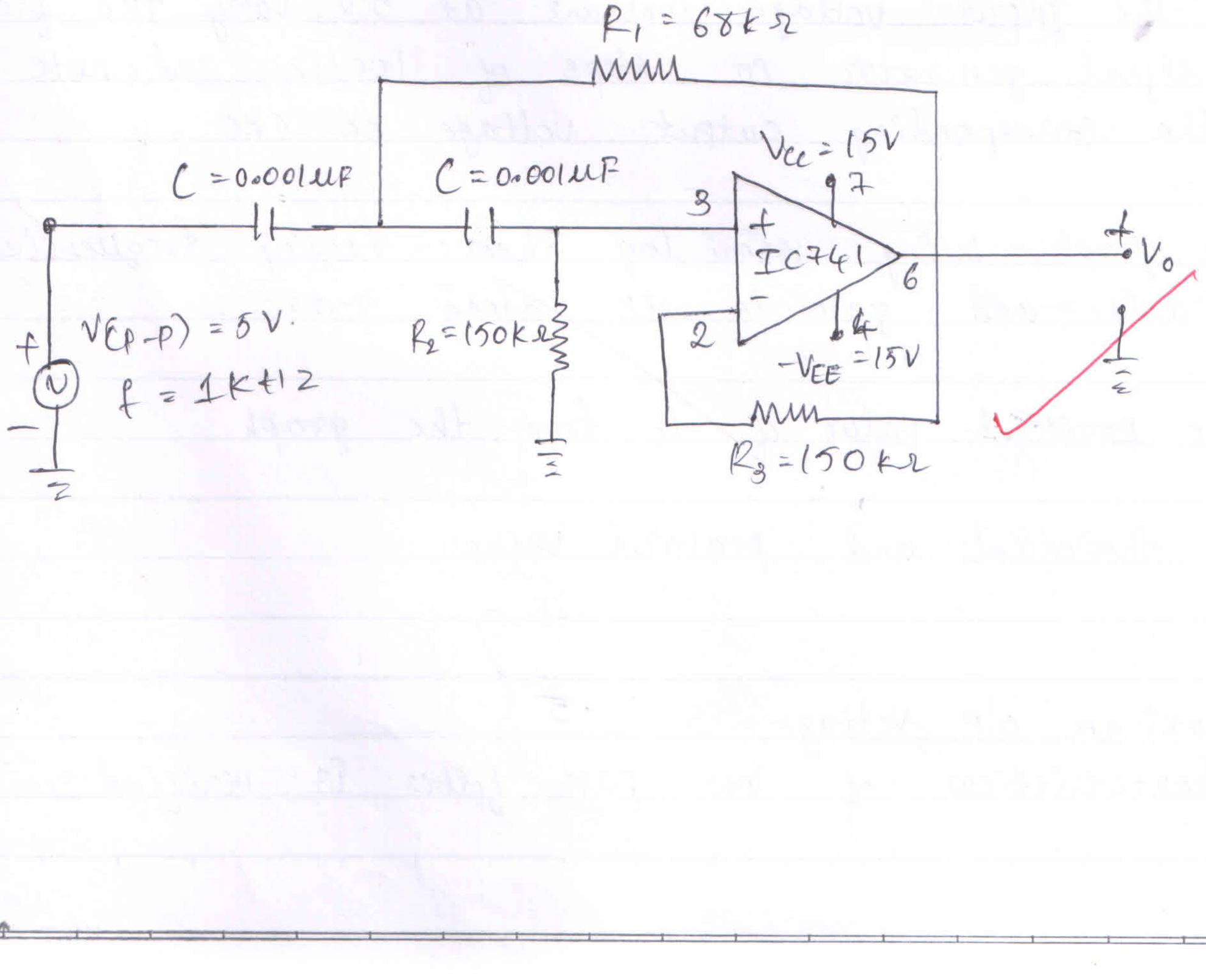
$$R_1 = \frac{R_2}{2} = 70\ k\Omega \text{ (use } 68\ k\Omega \text{ standard value).}$$

$R_2 = \sqrt{2}\,C_1$ at $f_c = 1.5$ kHz.

$$C_2 = \frac{\sqrt{2}}{2\pi f_c R_2} = \frac{\sqrt{2}}{2\pi \times 1.5\times10^3 \times 150\times10^3} = 1\ nF$$

$C_2 = 0.001\ \mu F$

Second order High Pass Filter.



(b) Second Order Active High-Pass Filters.

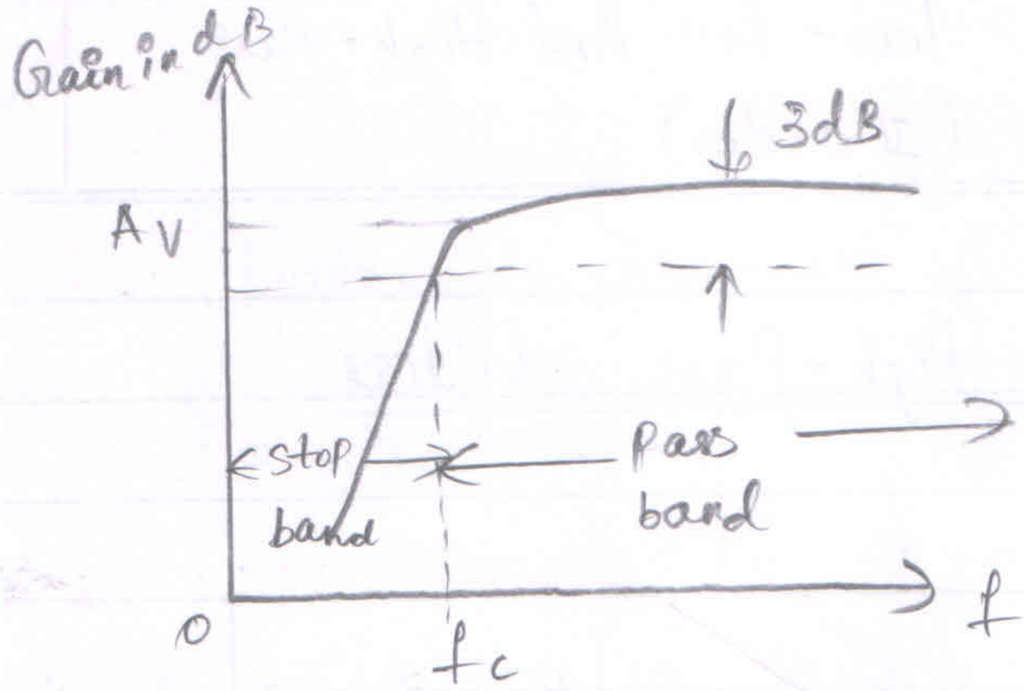
Components Required

Sl. No	Components	Quantity	
1	Regulated Power Supply ±15V	1	
2.	Function Generator	1	
3	CRO	1	
4	IC741	1	
5	Resistors :		
	68kΩ	1	
	150kΩ	2	
	0.001μF	2	
6	Bread board, Connecting Wires	1 set	

Theory :-

High pass filters attenuate the output voltage for all frequencies below the cut-off frequency fc. Above fc, the magnitude of the output voltage is constant. The range of frequencies that are transmitted is known as the pass band. The range of frequencies that are attenuated is known as the stop band.

High pass filters are often formed simply by inter-changing frequency determining resistors is formed and capacitors in low-pass filters. That is first-order high-pass filter is formed from a first order low-pass type by interchanging components R & C.



Expected frequency Response Curve.

Tabulation.

Input Voltage $V_{in} = 5V$.

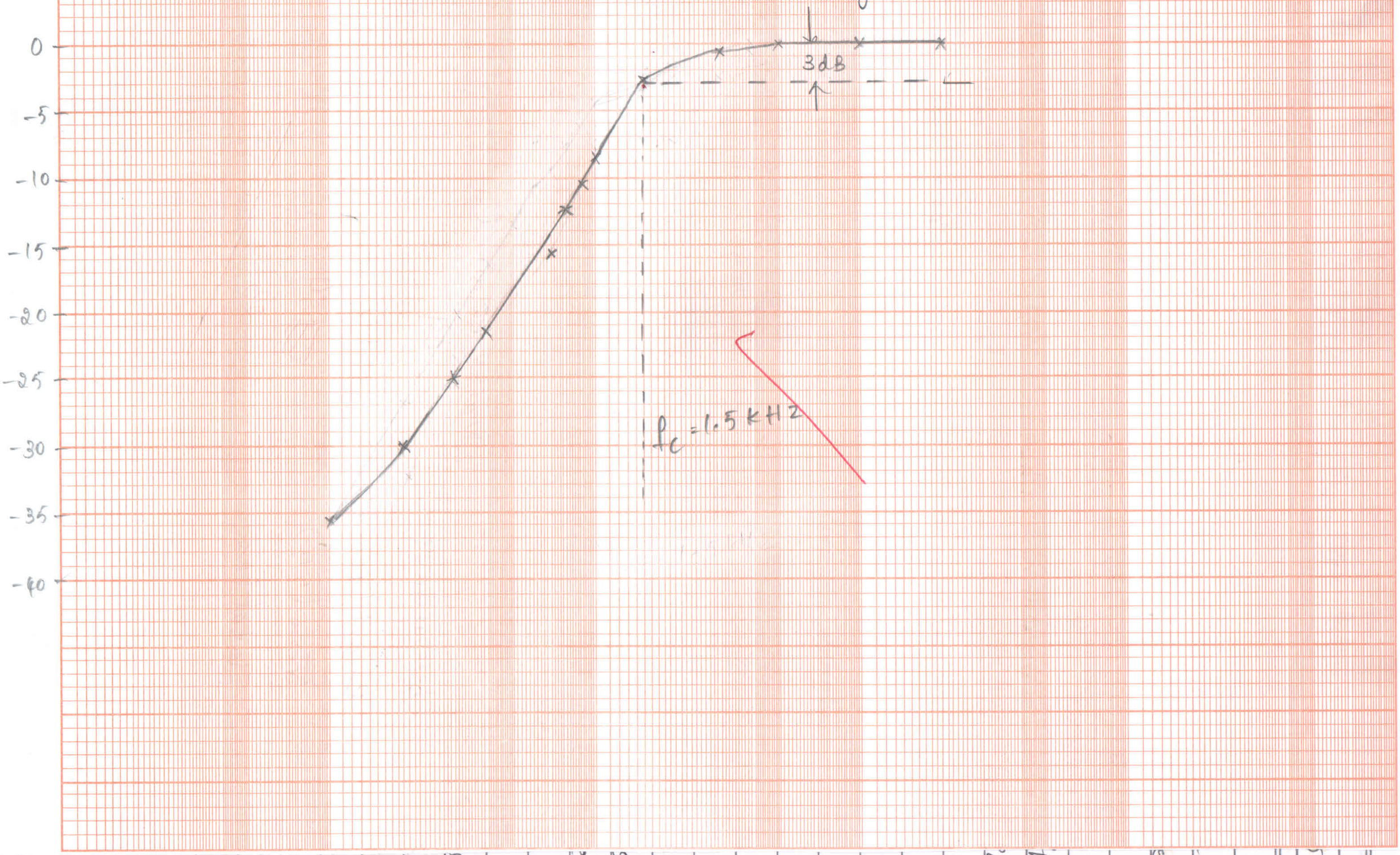
Frequency Hz.	o/p voltage V_o	Gain = V_o/V_i	Gain in dB = $20\log_{10}(V_o/V_i)$
100	0.080	0.016	-35.918
200	0.120	0.03	-30.458
300	0.280	0.056	-25.036
400	0.410	0.082	-21.724
500	0.560	0.084	-21.514
600	0.850	0.17	-15.391
700	1.14	0.228	-12.841
800	1.4	0.28	-11.057
900	1.8	0.36	-8.874
1k	2.2	0.44	-7.131
1.5k	3.6	0.72	-2.853
2k	4.8	0.96	-0.355
3k	5	1	0
4k	5	1	0
5k	5	1	0
10k	5	1	0
20k	5	1	0

Observation :

V_o = 3.6 V at f_c = 1.5 KHz

High Pass filter	Cut off frequency (theoretical) $f_c = 1.5$ kHz	Cut off frequency (Practical) $f_c = 1.5$ kHz

Second Order Active High Pass Filter



	Marks obtained
Observation (10 M)	09
Record (10M)	10
Viva (5 M)	~~09~~ 04
Total (25)	23

DATE 13/02/19
EXP. NO. 1

EXPT. TITLE : Active low-Pass And High-Pass Filters (II order)

Figure shows a first order high pass butterworth filter with a low cut off frequency of fc. This is the frequency at which the magnitude of the gain is a 0.707 times its pass band value. Obviously, all frequencies higher that f_c are pass band frequencies, with the highest frequency determined by the closed-loop bandwidth of the op-amp.

Procedure :-

Rig up the circuit as shown in circuit diagram

Initially keep the Input voltage $V_{in} = 5V$ constant at a frequency of 1.5 kHz.

Vary the frequency of the signal generator in steps of 100 Hz keeping Input Voltage constant at 5V and note down the corresponding output waveform on CRO.

Plot the graph using semi log sheet taking frequencies along x-axis and gain in dB along y-axis.

Find the practical value of f_c from the graph.

Compare theoretical and practical values.

Result :-

The maximum o/p voltage is 5

Thus, characteristics of high pass filter is verified.

20/2/19

Design

Let the Oscillating frequency of RC phase shift Oscillator $f_o = 2895$ Hz.

$I_1 \ggg I_{BMax}$

$I_{BMax} = 500$ nA (741)

$I_1 = 50\,\mu A$

$V_o = \pm (V_{cc} - 1) \approx \pm (15 - 1) = \pm 14$ V.

$R_2 = \frac{14}{50\,\mu A} = 280$ kΩ (220 kΩ standard Value to be used)

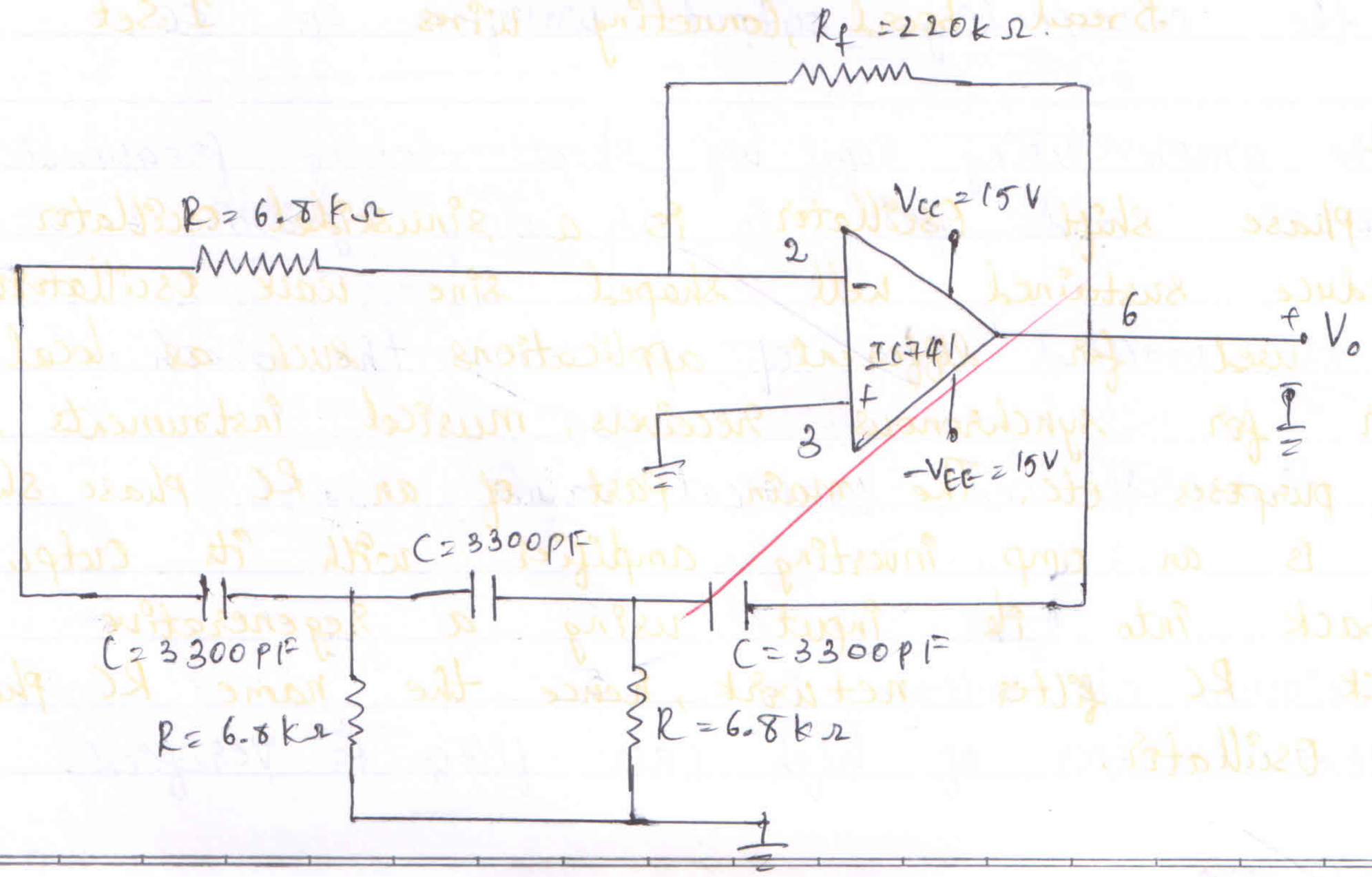
$R_1 = \frac{R_2}{A_V} = \frac{220\,k\Omega}{29} = 7.6$ kΩ (6.8 kΩ standard value to be used)

Select $R = R_1 = 6.8$ kΩ.

$$C = \frac{1}{2\pi RC\sqrt{6}} = \frac{1}{2\pi \times 6.8 \times 10^3 \times 2895 \times \sqrt{6}}$$

$C = 3.3 \times 10^{-9}$ F = 3300 pF (Standard value)

RC Phase Shift Oscillator.



DATE 20/2/19
EXP. NO. 2

EXPT. TITLE : RC Phase shift Oscillator and Wein bridge Oscillator

PAGE NO. 6

Aim :-

To design a RC phase shift and Wein bridge Oscillator using op-amp for a given oscillating frequency.

(a) RC Phase shift Oscillator

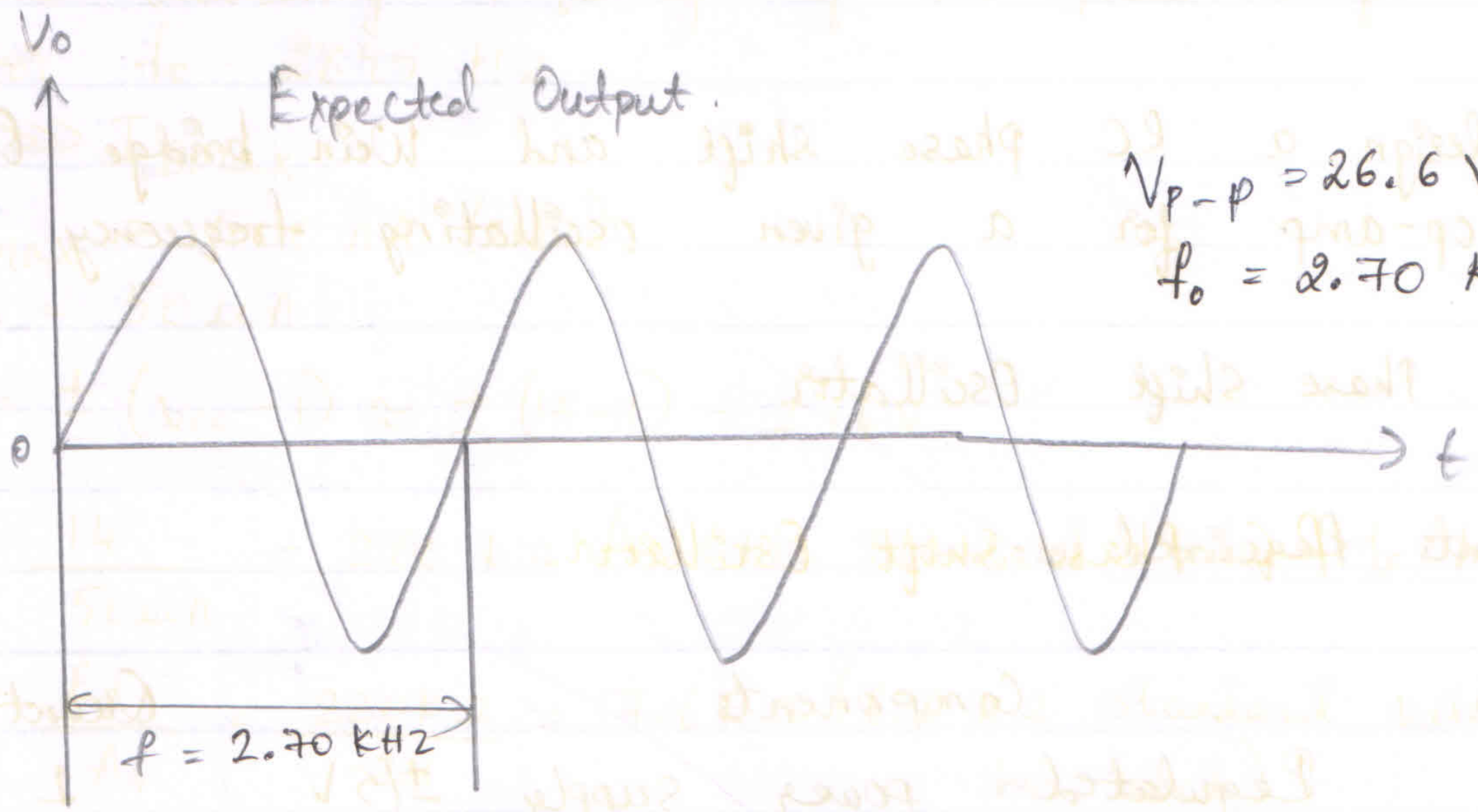
Components Required :

SI. No	Components	Quantity
1	Regulated power supply ±15V	1
2	CRO	1
3	IC 741	1
4	Resistors :	
	6.8 kΩ	3
	220 kΩ	1
	3300 pF	3
5	Bread board, Connecting wires	1 set

Theory :-

RC phase shift Oscillator is a sinusoidal oscillator used to produce sustained well shaped sine wave oscillators. It is used for different applications such as local Oscillator for synchronous receivers, musical Instruments, study purposes etc. The main part of an RC phase shift Oscillator is an opamp inverting amplifier with its output fed back into its input using a regenerative feedback RC filter network, hence the name RC phase shift Oscillator.

Graph.



$V_{p-p} = 26.6\ V$

$f_o = 2.70\ KHz$

Observations

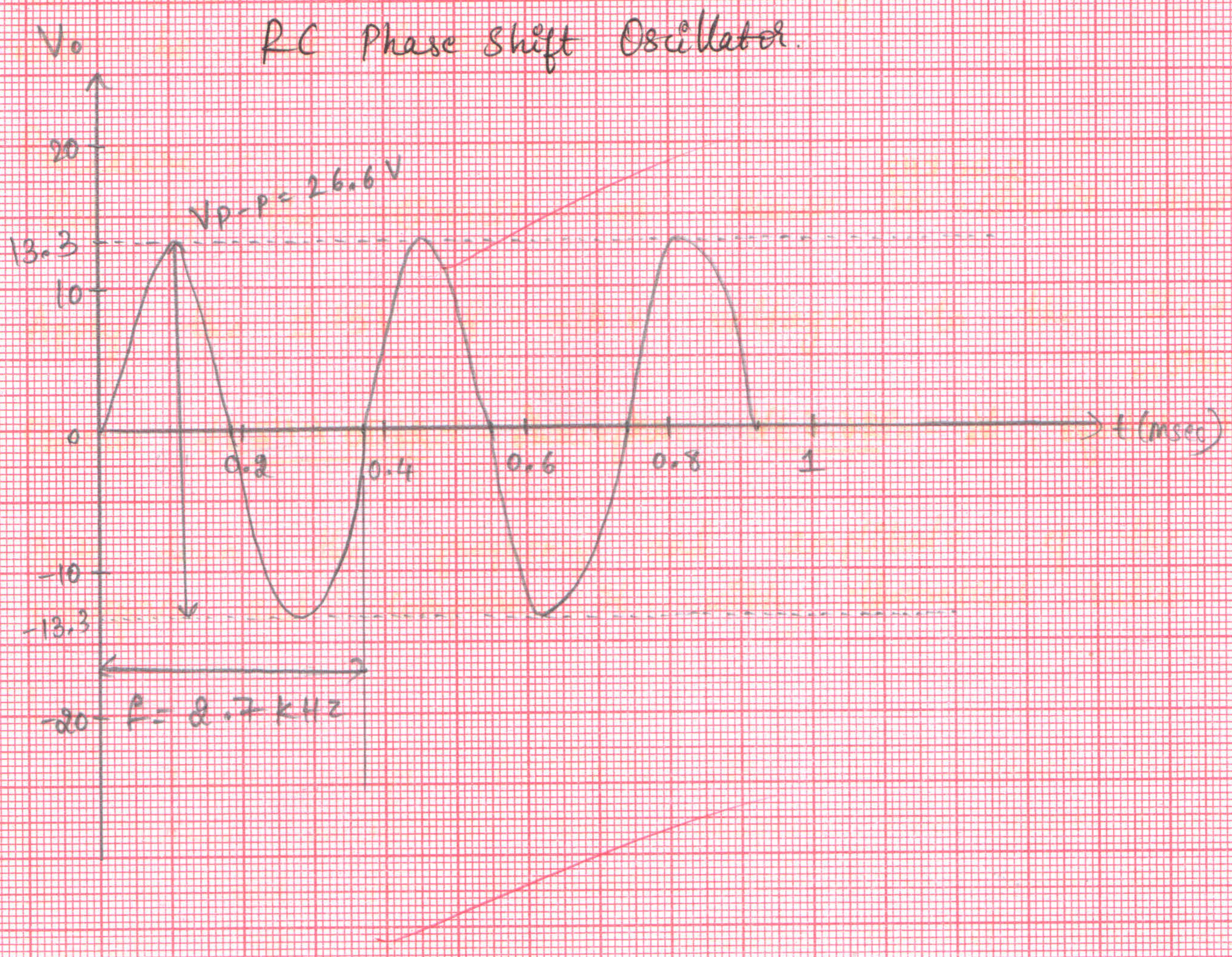
Output Voltage, $V_o =$ 26.6 V at $f_o =$ 2.70 KHz.

Scale :-

X-axis = 2cm = 0.2 msec

Y-axis = 2cm = 10 V.

RC Phase shift Oscillator.



By varying the capacitor, the frequency of oscillations can be varied. The feedback RC network has a phase shift of 60 degrees each, hence total phase shift provided by the three RC network is 180 degrees. The op-amp is connected as inverting amplifier hence the total phase shift around the loop will be 360 degrees.

Procedure :-

1. Rig up the circuit as shown in circuit diagram.
2. Apply the ±15V & −15V voltages to the IC741.
3. Observe the output waveform at pin no. 6.
4. Note down the frequency and amplitude of the output waveform and compare it with theoretical value.

Design :-

Let the frequency of Wein's bridge Oscillator = 15 kHz.

Select

$C_1 = C_2 = C = 0.01\ \mu F$.

$R = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 15\ kHz \times 0.01 \times 10^{-6}}$

$R = 1.06\ k\Omega$ (1 kΩ standard value to be used)

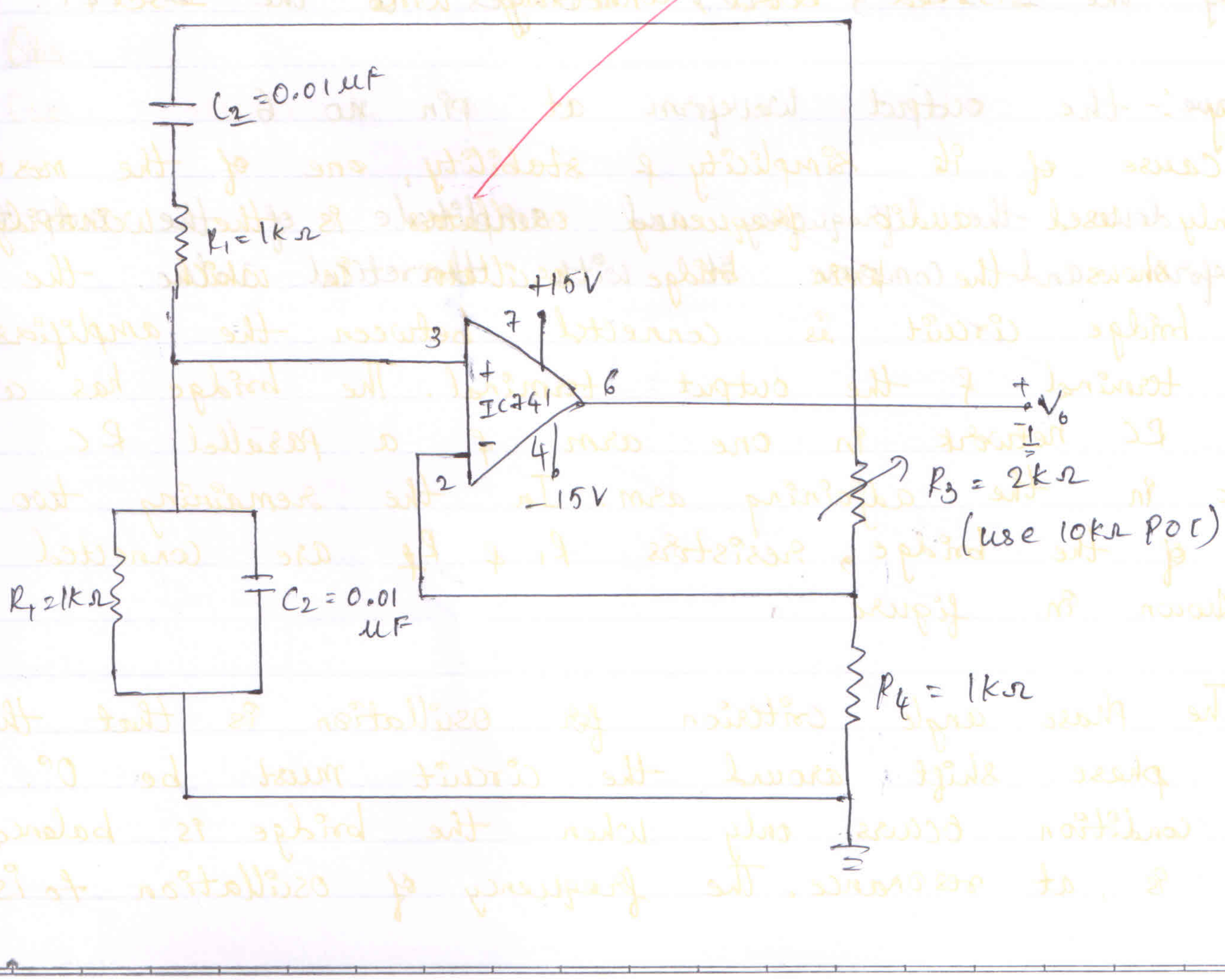
$R_1 = R_2 = R = 1\ k\Omega$.

let $R_4 = 1\ k\Omega$.

$A_V = 3$, $R_3 = 2R_4 = 2 \times 1\ k\Omega = 2\ k\Omega$.

Use 10 kΩ potentiometer.

Weins Bridge Oscillator



DATE 20/2/19

EXP. NO. 2

EXPT. TITLE : RC Phase shift Oscillator and Wein bridge Oscillator

PAGE NO. 8

(b) Wein bridge Oscillator

Components Requirement.

Sl. No	Components	Quantity
1	Regulated Power Supply ±15 V	1
2	CRO	1
3	IC741	1
4	Resistors :	
	0.01μF	2
	1 kΩ	3
	10 kΩ Pot	1
5	Bread board, Connecting wires	1 set

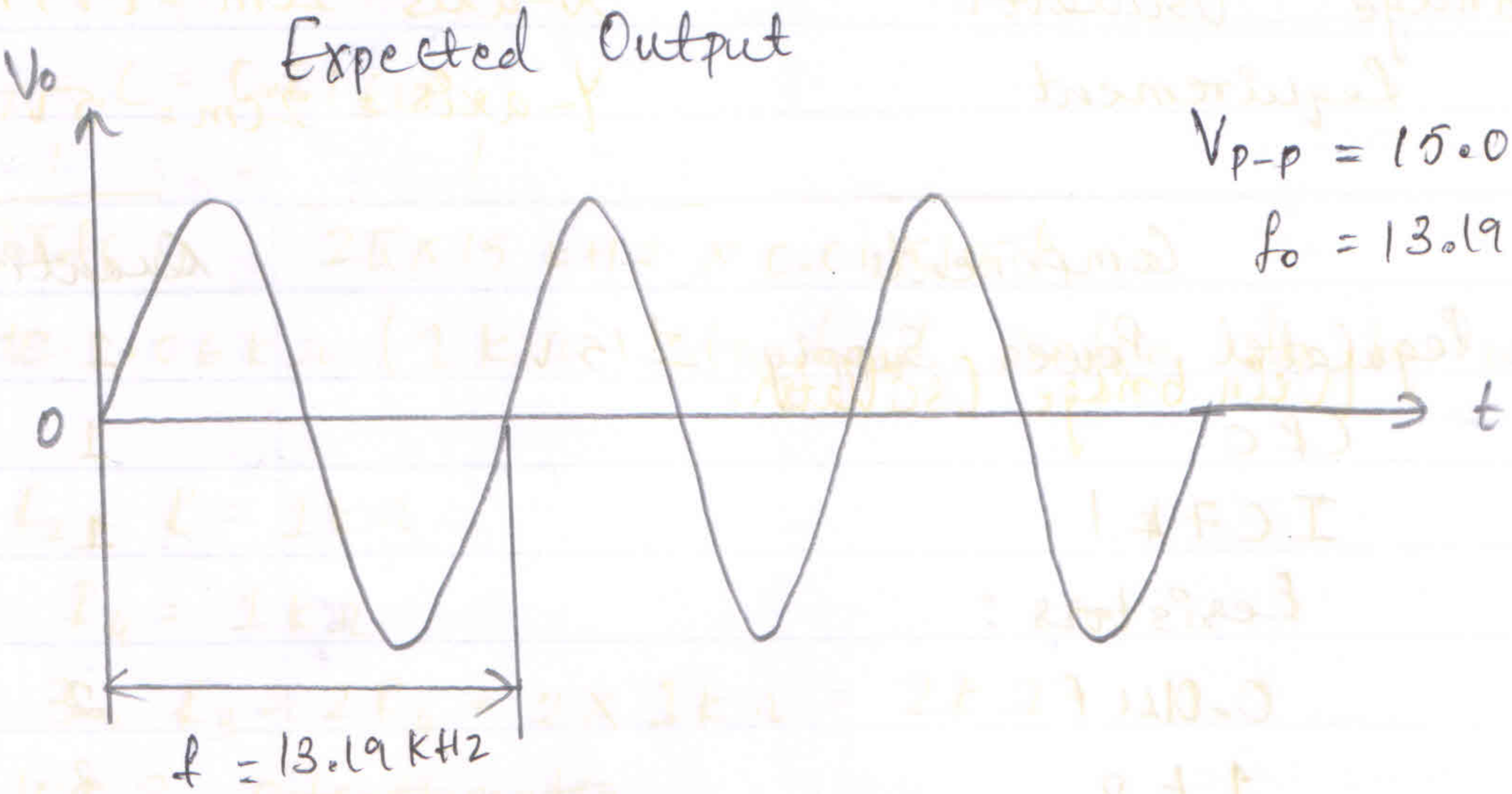
Theory :-

Because of its simplicity & stability, one of the most commonly used audio frequency oscillators is the Wein bridge. Figure shows the Wein bridge oscillator in which the wein bridge circuit is connected between the amplifiers input terminal & the output terminal. The bridge has a series RC network in one arm & a parallel RC network in the adjoining arm. In the remaining two arms of the bridge, resistors R_1 & R_f are connected as shown in figure.

The phase angle criterion for oscillation is that the total phase shift around the circuit must be 0°. This condition occurs only when the bridge is balanced, that is, at resonance. The frequency of oscillation f_o is

Graph

Expected Output



$V_{p-p} = 15.02\,V$.

$f_o = 13.19\,KHz$

Observation :-

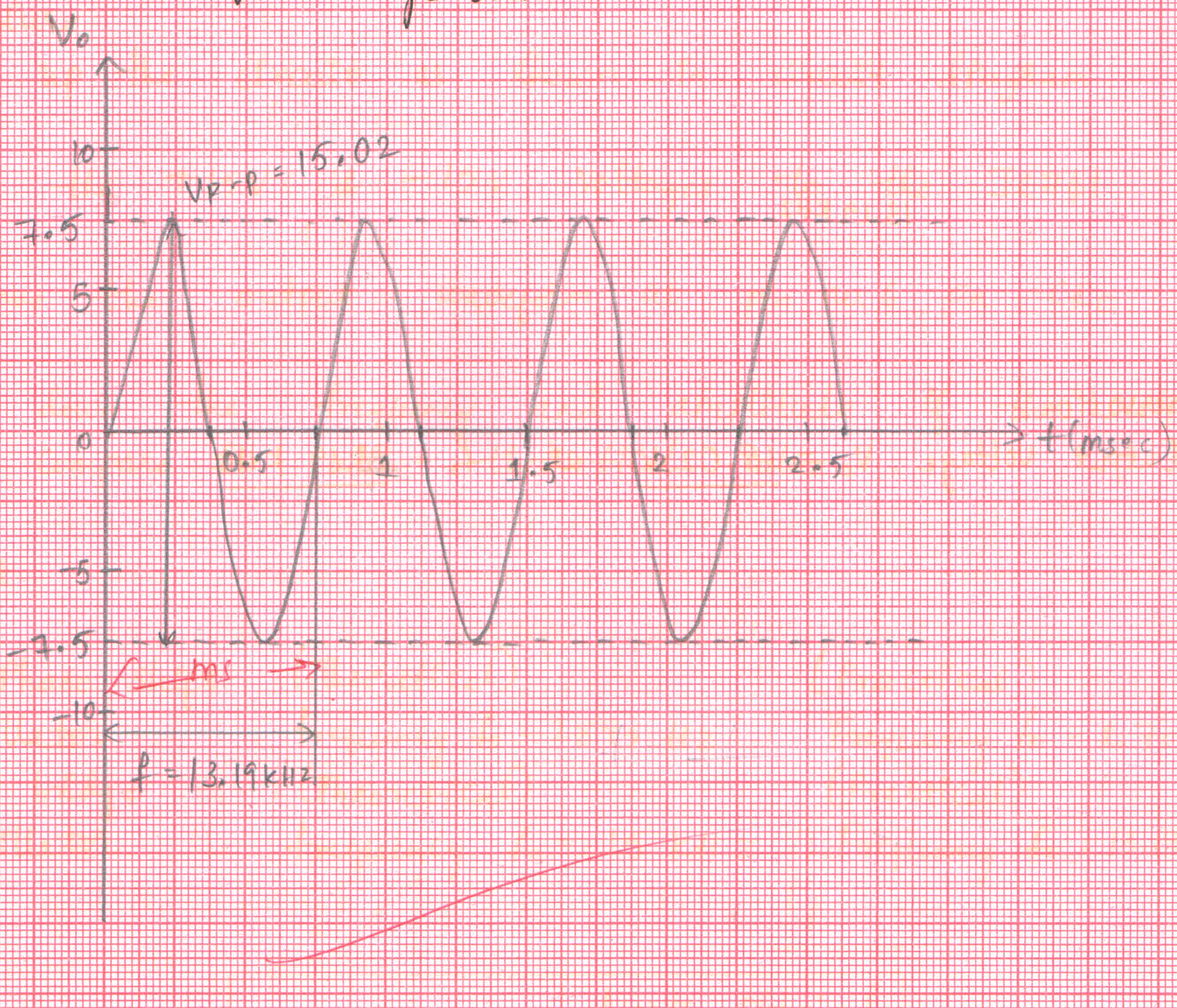
Output voltage, $V_o = \underline{15.02\,V}$ at $f_o = \underline{13.19\,KHz}$.

Scale :-

X-axis = 2cm = 0.5 msec.

Y-axis = 2cm = 5 V.

Wein bridge Oscillator.



exactly the resonant frequency of the balanced Wein bridge & is given by

$$f_o = \frac{1}{2\pi RC}$$

Procedure

Rig up the circuit as shown in circuit diagram.

Apply the +15V & -15V voltages to the IC741.

Observe the output waveform at pin no. 6 on CRO.

Note down the frequency and amplitude of the output and compare it with theoretical value.

Result

RC Phase shift Oscillator	(Theoretical) frequency f_o = 2895 Hz	(Practical) Frequency f_o = 2.70 KHz
Wein bridge Oscillator	(Theoretical) frequency f_o = 15 KHz	(Practical) frequency f_o = 13.19 KHz

	Marks obtained
Record (10)	10
Observation (10)	10
Viva (0)	3
Total (25)	23

Saluja
27/2/19

Design

Let Input voltage $V_i = 1.1V$.

In an inverting amplifier, $V_o = -(aV_1 + bV_2)$

where $a = b = 1$.

$I_{Bmax} = 500\,nA$, Let $V_1 = V_2 = 1.1V$.

$I_f = 100\, I_{Bmax} = 100 \times 50\,nA = 50\,\mu A$.

$V_o = -(aV_1 + bV_2)$.

Let $a = b = 1$ for adder.

$R_1 = \frac{V_i}{I_f} = \frac{1.1}{50\,\mu A} = 22\,k\Omega$.

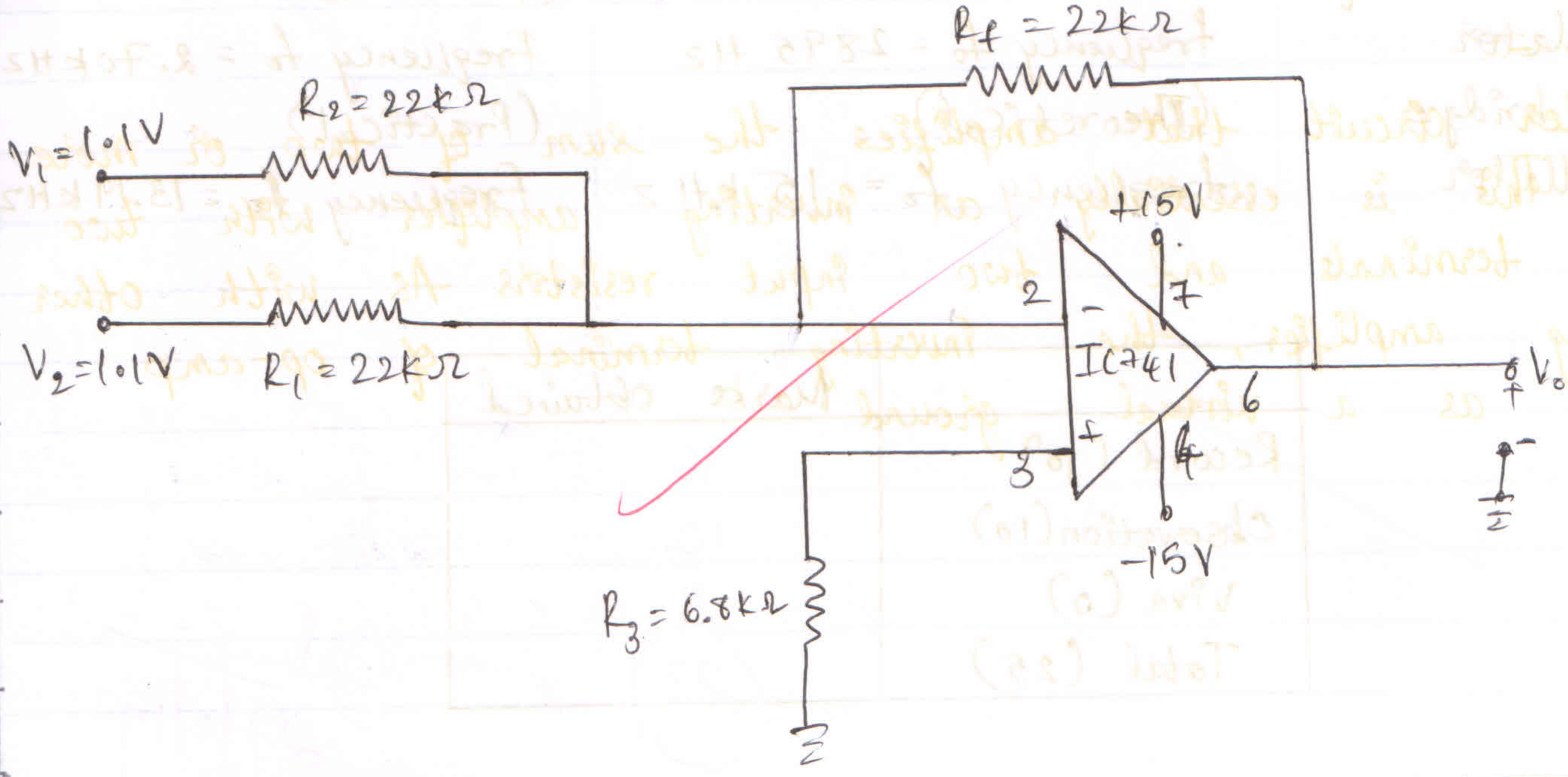
$R_1 = R_2 = R_f = 22\,k\Omega$ (std value)

$R_3 = R_1 \| R_2 \| R_f = 7.333\,k\Omega$ use $6.8\,k\Omega$.

$V_o = -(V_1 + V_2) = V_1 = V_2 = 1.1V$.

ADDER

Inverting Summing Amplifier.



DATE 20/2/19

EXP. NO. 3

EXPT. TITLE : Adder, Integrator and Differentiator

PAGE NO. 10

Aim :-

To design an ADDER circuit using op-amp 741 and verify its working demonstrate an experiment for Adder, differentiator and Integrator.

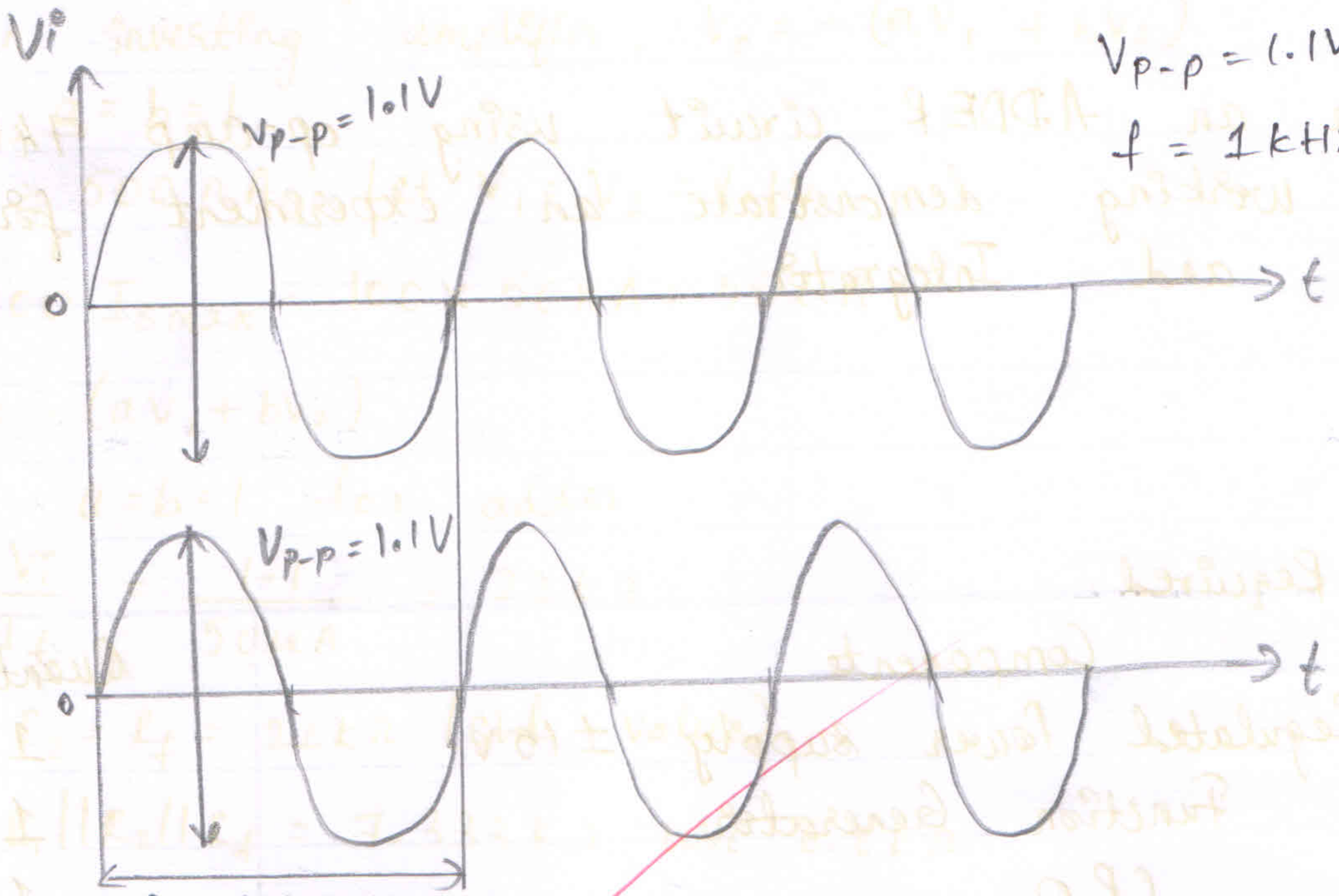
(a) ADDER.

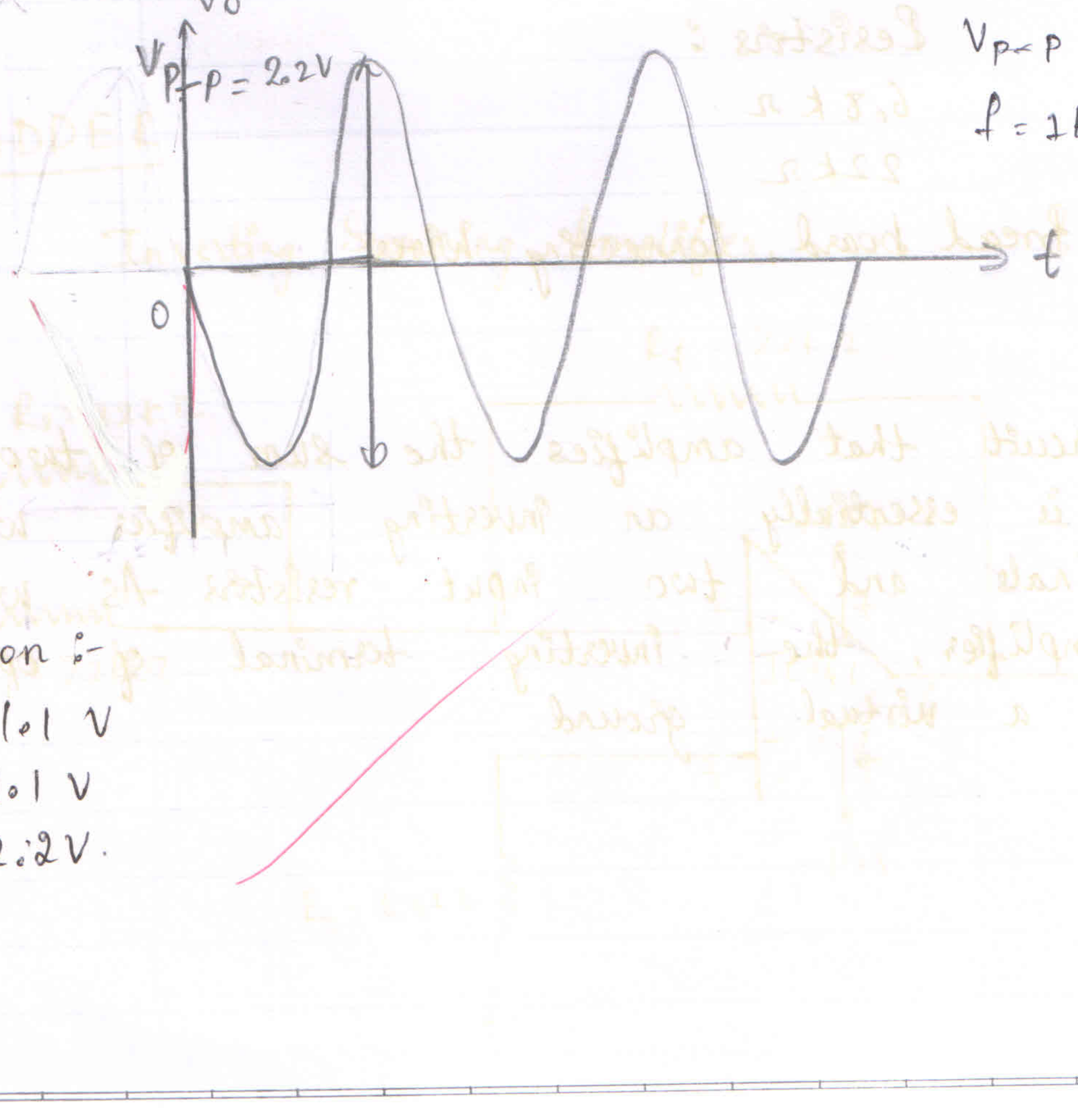
Components Required.

Sl. No	Components	Quantity
1	Regulated Power supply ±15V	1
2	Function Generator	1
3	CRO	1
4	IC741	1
5	Resistors :	
	6.8 kΩ	1
	22kΩ	3
6	Bread board, Connecting wires	1 set

Theory -

Adder circuit that amplifies the sum of two or more inputs. This is essentially an inverting amplifier with two input terminals and two input resistors. As with other inverting amplifier, the inverting terminal of op-amp behaves as a virtual ground.





Observation :-

$V_1 = 1.1\ V$

$V_2 = 1.1\ V$

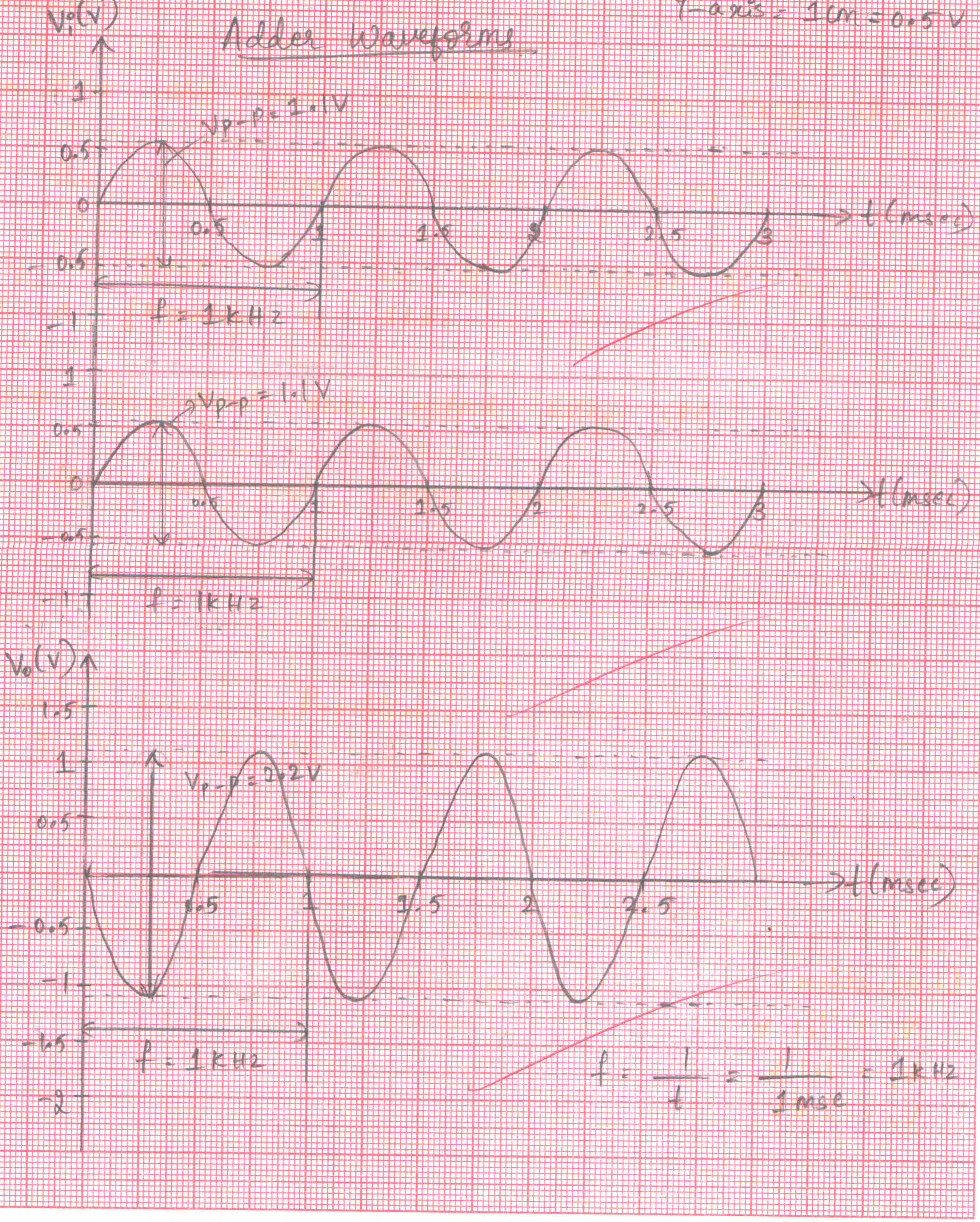
$V_o = 2.2V.$

Adder Waveforms

Scale :-

X-axis = 2 cm = 0.5 msec

Y-axis = 1 cm = 0.5 V



DATE 20/2/19
EXP. NO. 3

EXPT. TITLE : Adder, Integrator and Differentiator

PAGE NO. 11

Procedure -

Connections are made as shown in the circuit diagram.

Set the power supply to +15 V and −15 V

Apply ac input sine wave of amplitude of $V_1 = V_2 = 1.1$ V and a frequency of 1KHz.

Observe the input and output using CRO.

Plot the input and output waveforms.

Result :-

Theoretical	Practical
$V_o = 2.2$ V	$V_o = 2.2$ V

Design.

Let $V_o = 5V$, Select a ramp input with amplitude 1V for a frequency of 5KHZ.

$I_1 \ggg I_{B(max)}$

Let $I_1 = 500\mu A$.

$$R_2 = \frac{V_o}{I_1} = \frac{5V}{500\mu A} = 10k\Omega \text{ (std. value)}$$

$$C_1 = \frac{I_1 \times \Delta t}{\Delta V} = \frac{500\mu A \times 100\mu s}{1V}$$

$C_1 = 0.05\mu F$ (std. value)

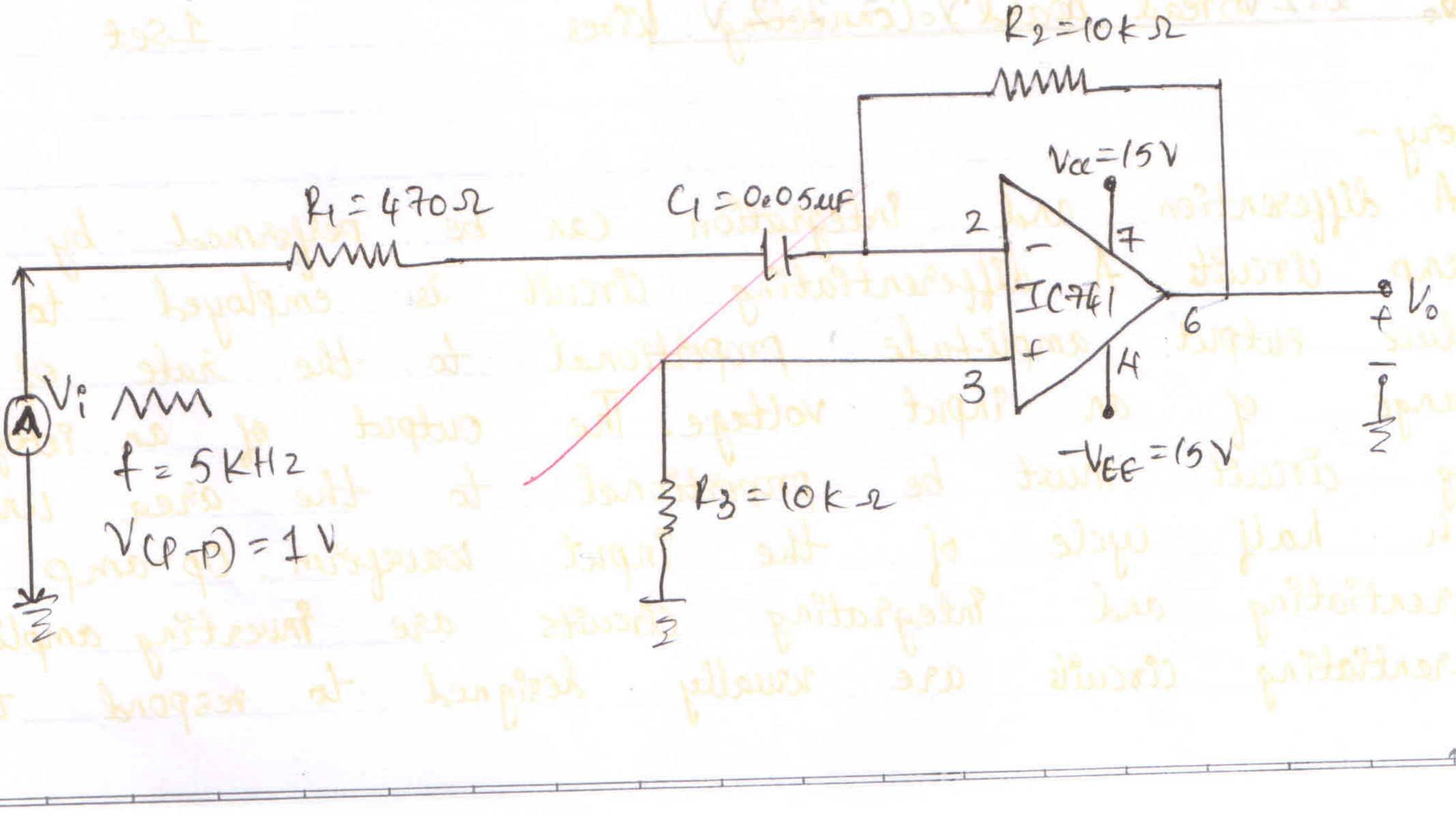
$$R_1 = \frac{R_2}{20} = \frac{10k\Omega}{20} = 500\Omega \text{ (use } 470\Omega \text{ std value)}$$

$R_3 = R_2 = 10k\Omega$.

$V_{cc} \geq \pm (V_o + 3V) = \pm(5V + 3V)$

$V_{cc} \geq \pm 8V$.

Differentiator



DATE 20/2/19
EXP. NO. 3

EXPT. TITLE : Adder, Integrator and Differentiator

(b) Differentiator and Integrator.

Aim :-

Design a differentiator and integrator using operational amplifier 741 and verify its working.

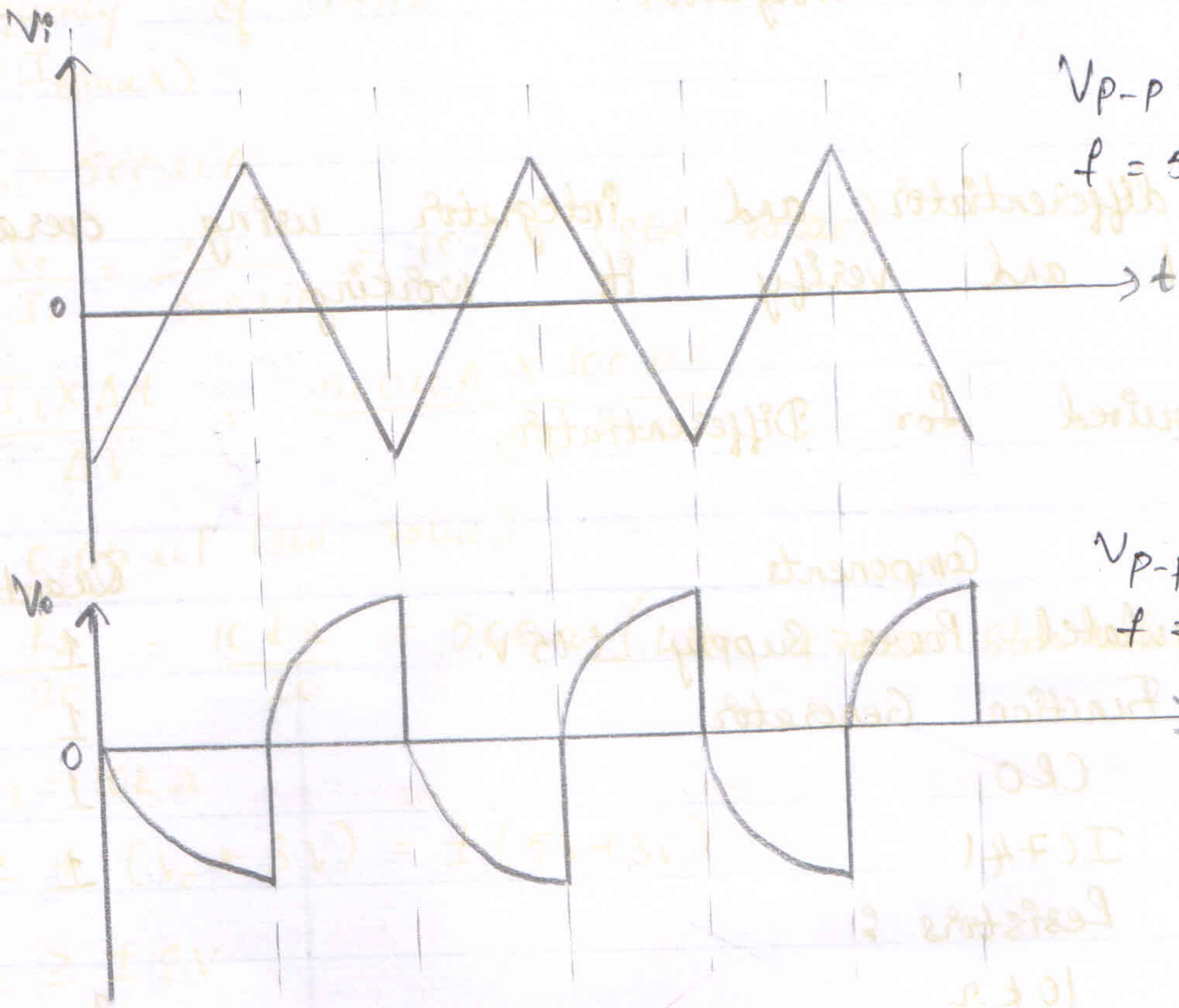
Components required for Differentiator.

Sl. No	Components	Quantity
1	Regulated Power Supply ±15 V.	1
2	Function Generator	1
3	CRO	1
4	IC741	1
5	Resistors &	
	10 kΩ	2
	470 kΩ	1
	0.05 μF	1
6	Bread board, Connecting Wires	1 set

Theory -

A differention and integration can be performed by op-amp circuits. A differentiating circuit is employed to produce output amplitude proportional to the rate of change of an input voltage. The output of an integrating circuit must be proportional to the area under each half cycle of the input waveform. Op-amp differentiating and integrating circuits are inverting amplifiers. Differentiating circuits are usually designed to respond to

Differentiator output waveform for Ramp wave input.

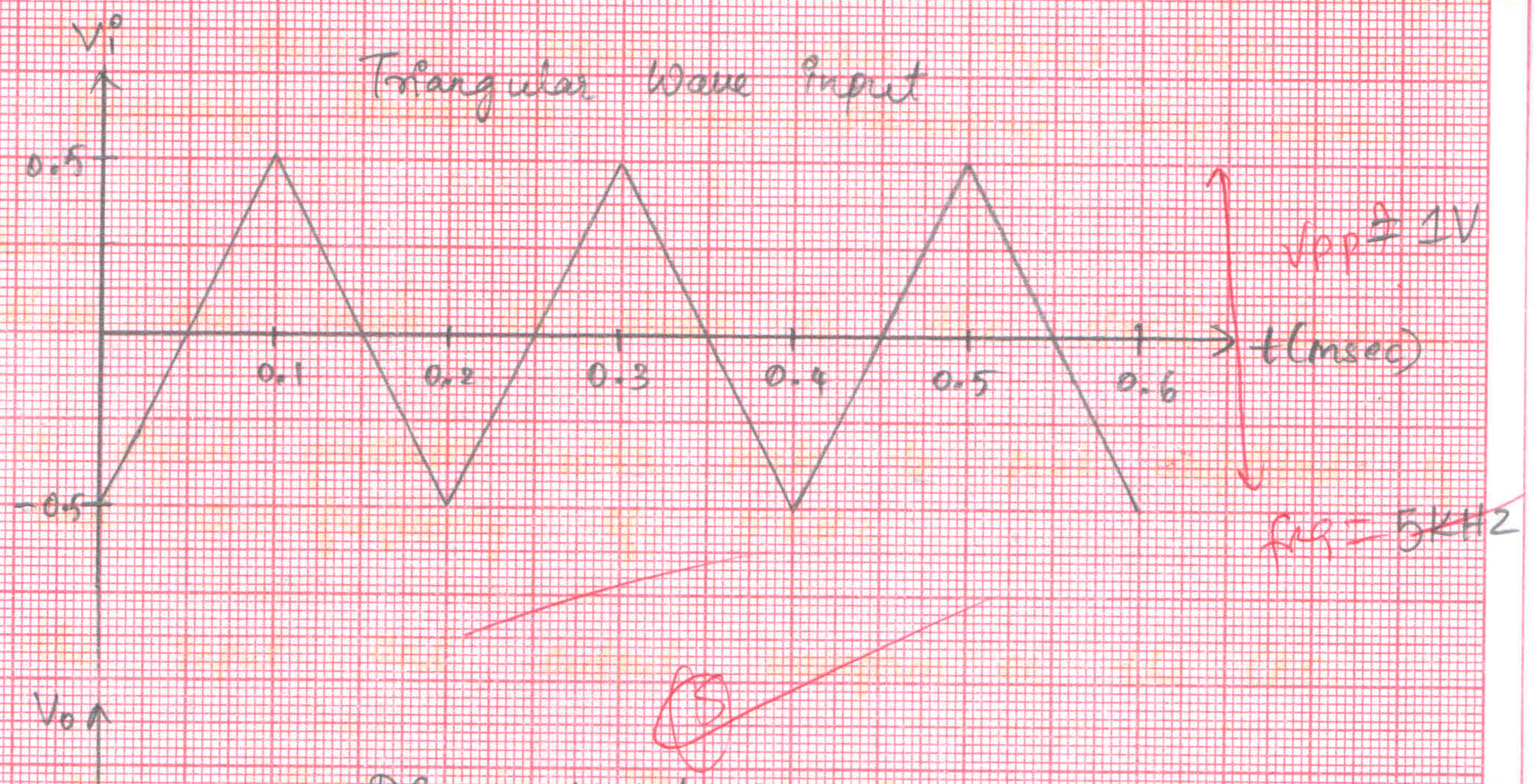


Scale:-

X-axis = 2cm = 0.1 msec

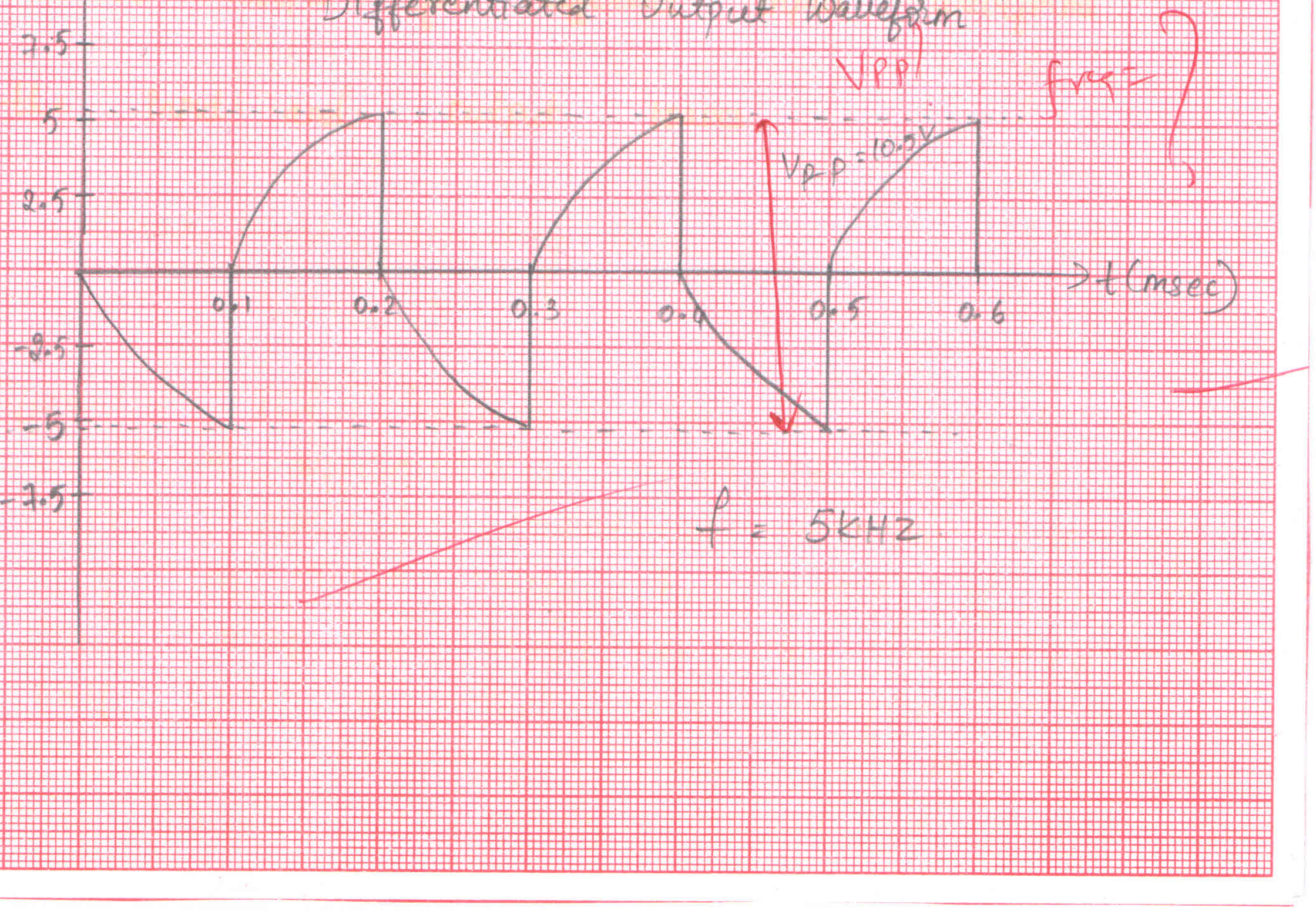
Y-axis = 2cm = 0.5 V

Triangular Wave Input



(S)

Differentiated Output Waveform



triangular and rectangular input waveforms. While integrating circuits are most often designed to produce a triangular wave output from a square wave input. Both circuits have frequency limitations when processing sine waves.

Procedure.

1. Connections are made as shown in the circuit diagram.
2. Set a signal generator with peak to peak amplitude of 1V and a frequency of 5 KHz.
3. Note the input and output waveform on the CRO.
4. Repeat above steps for different input waveforms.
5. Plot the input and output waves.

Design

For $V_{o(p-p)} = 4V$, $V_{i(p-p)} = 10V$.

$f_{in} = 500Hz$.

$C_1 >>>$ Stray capacitance.

Let $C_1 = 0.1\mu f$ (standard value)

$$\Delta t = \frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 500Hz} = 1ms.$$

$\Delta V = 4V$.

$$I_1 = \frac{C_1 \Delta V}{\Delta t} = \frac{0.1\mu f \times 4V}{1ms} = 400\mu A.$$

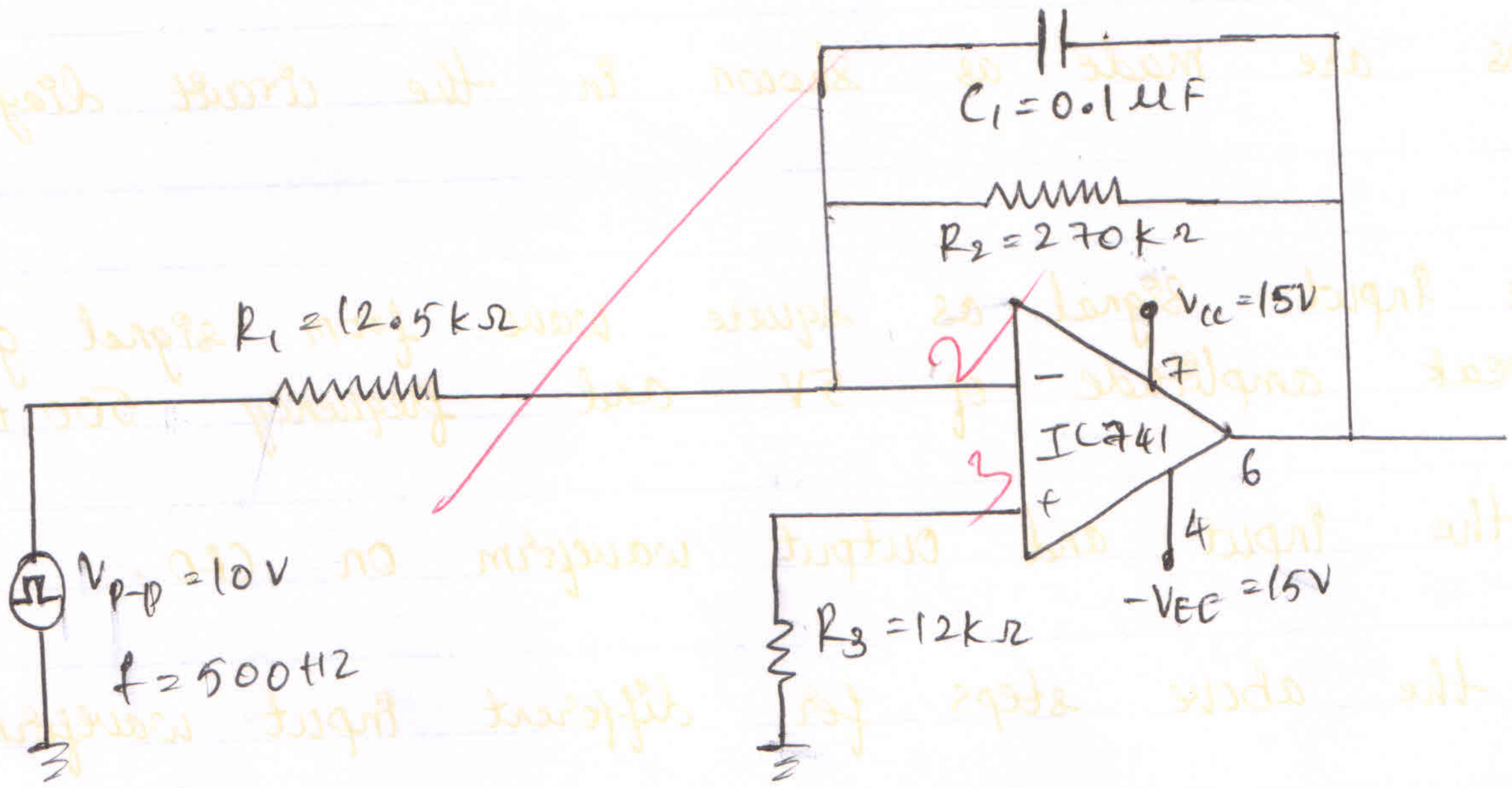
$$R_1 = \frac{V_i}{I_1} = \frac{5V}{400\mu A} = 12.5\ K\Omega.$$

$R_2 = 20R_1 = 20 \times 12.5\ k\Omega$.

$R_2 = 250\Omega$ (use a $270k\Omega$ standard value)

$R_3 = R_1 = 12.5k\Omega$ (use a $12k\Omega$ standard value)

Integrator



DATE 20/2/19 | EXPT. TITLE : Adder, Integrator and Differentiator. | PAGE NO. 14

EXP. NO. 3

(c) Integrator.

Components Requirement for Integrator:

SI. NO	Components	Quantity
1	Regulated Power Supply ±15V	1
2	Function generator	1
3	CRO	1
4	IC741	1
5	Resistors:	
	12kΩ	2
	270kΩ	1
	0.1μF	1
6	Bread board, Connecting Wires	1 set

Procedure

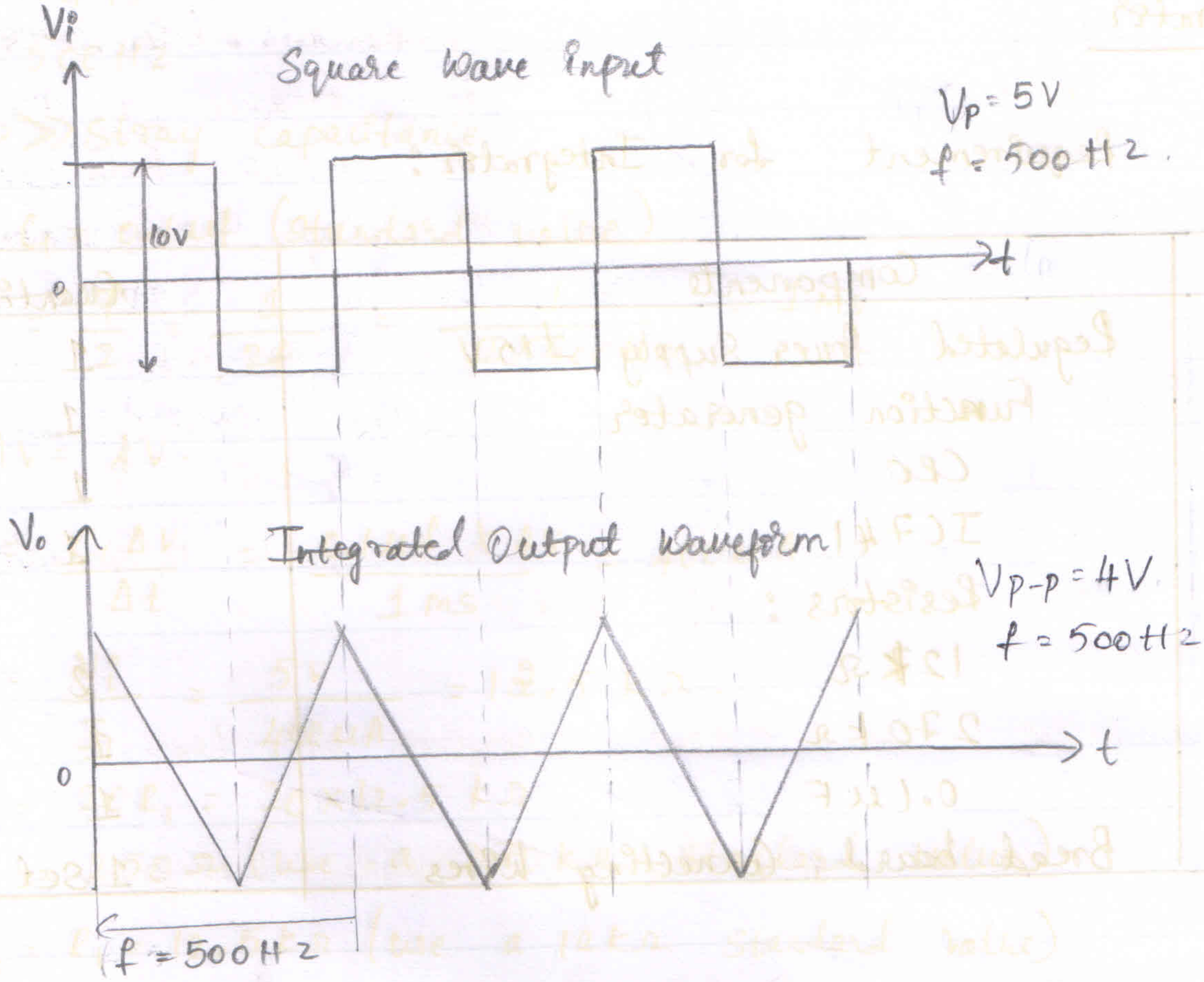
Connections are made as shown in the circuit diagram of fig.

Set the Input signal as square wave from signal generator with peak amplitude of 5V and frequency 500 Hz.

Note the input and output waveform on CRO.

Repeat the above steps for different Input waveforms.

Graph.

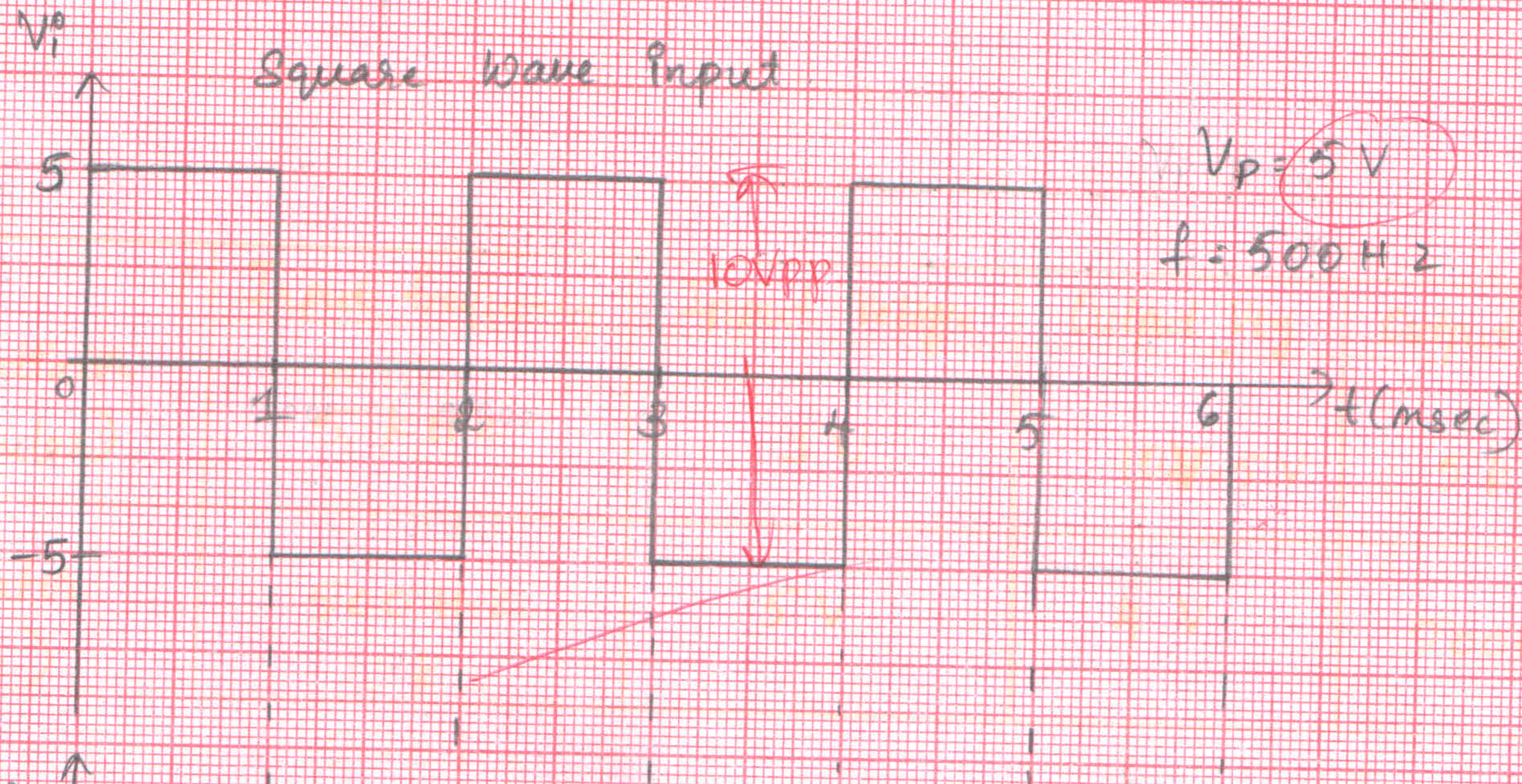

Vi
Square wave Input
Vp = 5V
f = 500Hz.
10V
0
t
Vo
Integrated Output Waveform
Vp-p = 4V
f = 500Hz.
0
t
f = 500Hz

Scale :-

X-axis = 2Cm = 1 msec

Y-axis = 2Cm = 5 V

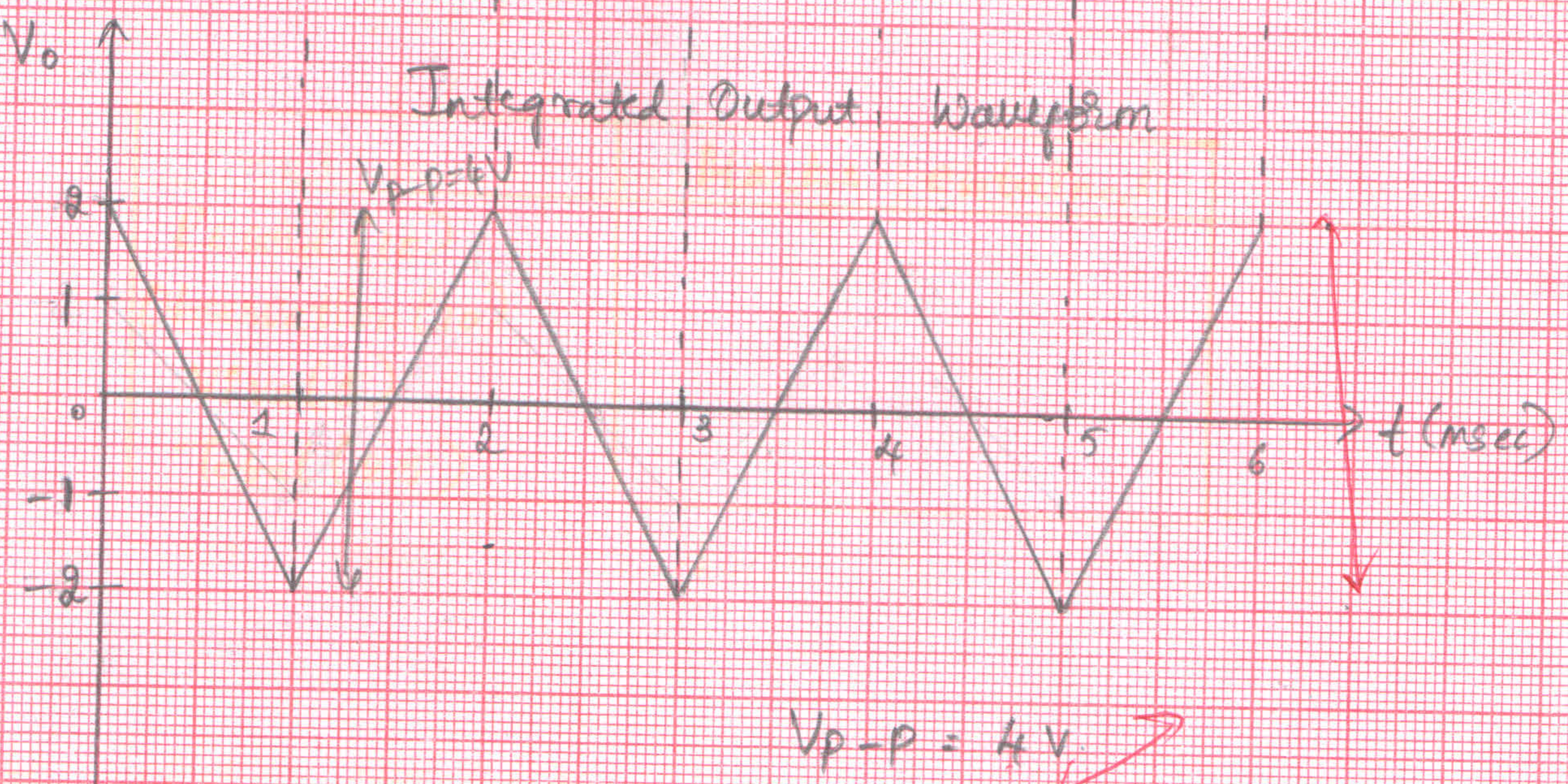
Square Wave Input



$V_p = 5$ V

$f = 500$ Hz

Integrated Output Waveform



$V_{p-p} = 4$ V

$f = \frac{1}{t} = \frac{1}{2\,msec} = 500$ Hz

DATE 20/2/19

EXP. NO. 3

EXPT. TITLE : Adder, Integrator and Differentiator

Plot the Input and output waveforms.

Result.

Diff	Input frequency	Input Voltage	Output Vtg	Output frequency
Differentiator (Triangular)	5 kHz	1 V	10.5 V	5 kHz
Integrator (Square)	500 Hz	5 V	4 V	500Hz

	Marks obtained
Record (10)	9
Observation (10)	10
Viva (5)	4
Total (25)	23

Salma
27/2/19

Design for 0.5 Volts step size.

To generate analog signals from binary BCD input for a given step voltage with LSB = 0.5V. The full scale analog output required for a DAC is 5V. The digital word available is at 4 bits.

$$V_o = \frac{V_R}{2^n}(2^0 B_0 + 2^1 B_1 + 2^2 B_2 + 2^3 B_3)$$

Where B_0, B_1, B_2, B_3 are binary i/p's.

Design for full scale output voltage of 5 volts.

$$V_o = \frac{V_R}{2^n}(2^0 B_0 + 2^1 B_1 + 2^2 B_2 + 2^3 B_3)$$

When all bits are high is $B_0\ B_1\ B_2\ B_3 = 5V$ [maximum]

Then $V_o = 3V$

$$3V = \frac{V_R}{24}(2^0 + 2^1 + 2^2 + 2^3)$$

$$3V = \frac{V_R}{16} \times 15.$$

$$V_R = \frac{3 \times 16}{15} = 5.33V.$$

$$V_R = 3.2V$$

DATE 27/2/19 | EXPT. TITLE : Digital to analog Converter | PAGE NO. 16

EXP. NO. 4

Aim :-

To design and construct a 4-bit R-2R Op-amp digital to analog converter using 4-bit binary input from toggle switches and Mod-16 Counter.

(a) Digital to Analog Converter using toggle switches.

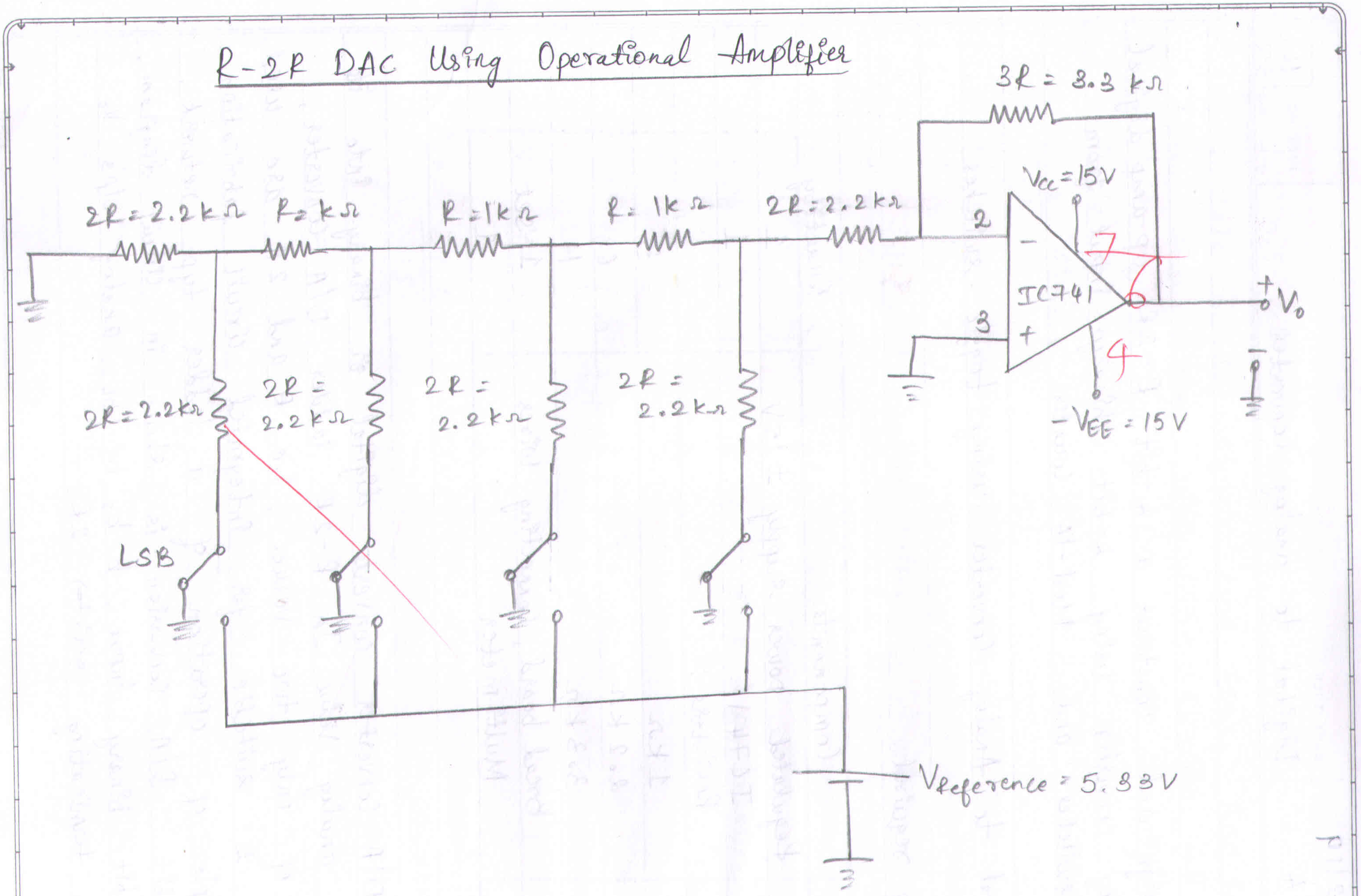
Components required.

Sl.No	Components	Quantity
1	Regulated power supply ±15V	1
2	IC741	1
3	Resistors :	
	1 kΩ	3
	2.2 kΩ	6
	3.3 kΩ	1
4	Bread board, Connecting Wires	1 set
5	Multi-meter	1

Theory :-

The D/A Converter converts digital or binary into its equivalent analog value. In R-2R ladder D/A Converter, resistors of only two values, i.e, R and 2R are used. Hence, it is suitable for integrated circuit fabrication. The principle of operation of a ladder type network, for 4-bit D/A Conversion is shown in circuit diagram, with 4-bit binary input, b_1 b_2 b_3 b_4, analog o/p's V_o and one terminating resistor 2R.

R-2R DAC Using Operational Amplifier



DATE 27/2/19

EXP. NO. 4

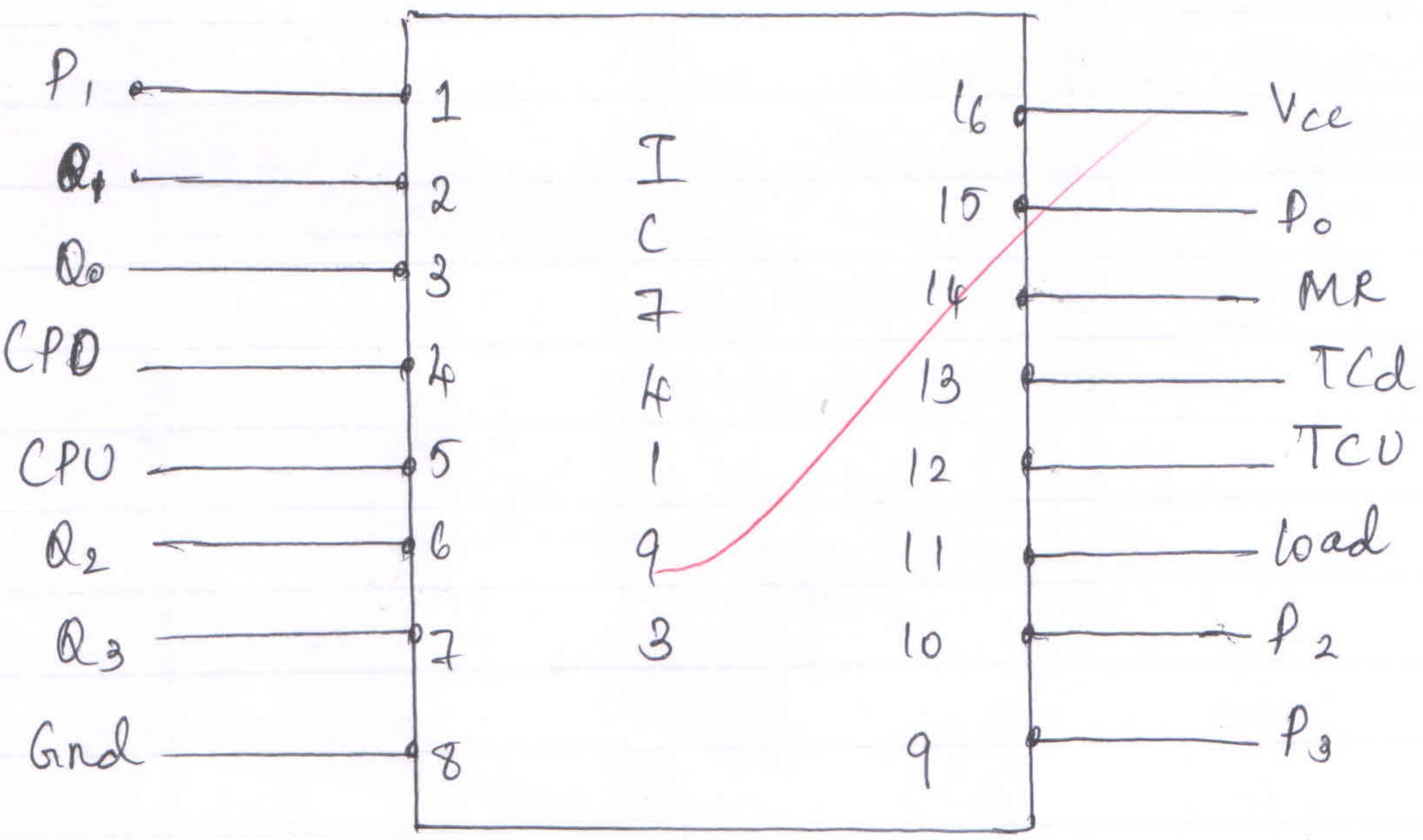
EXPT. TITLE : Digital to Analog Converter

Procedure

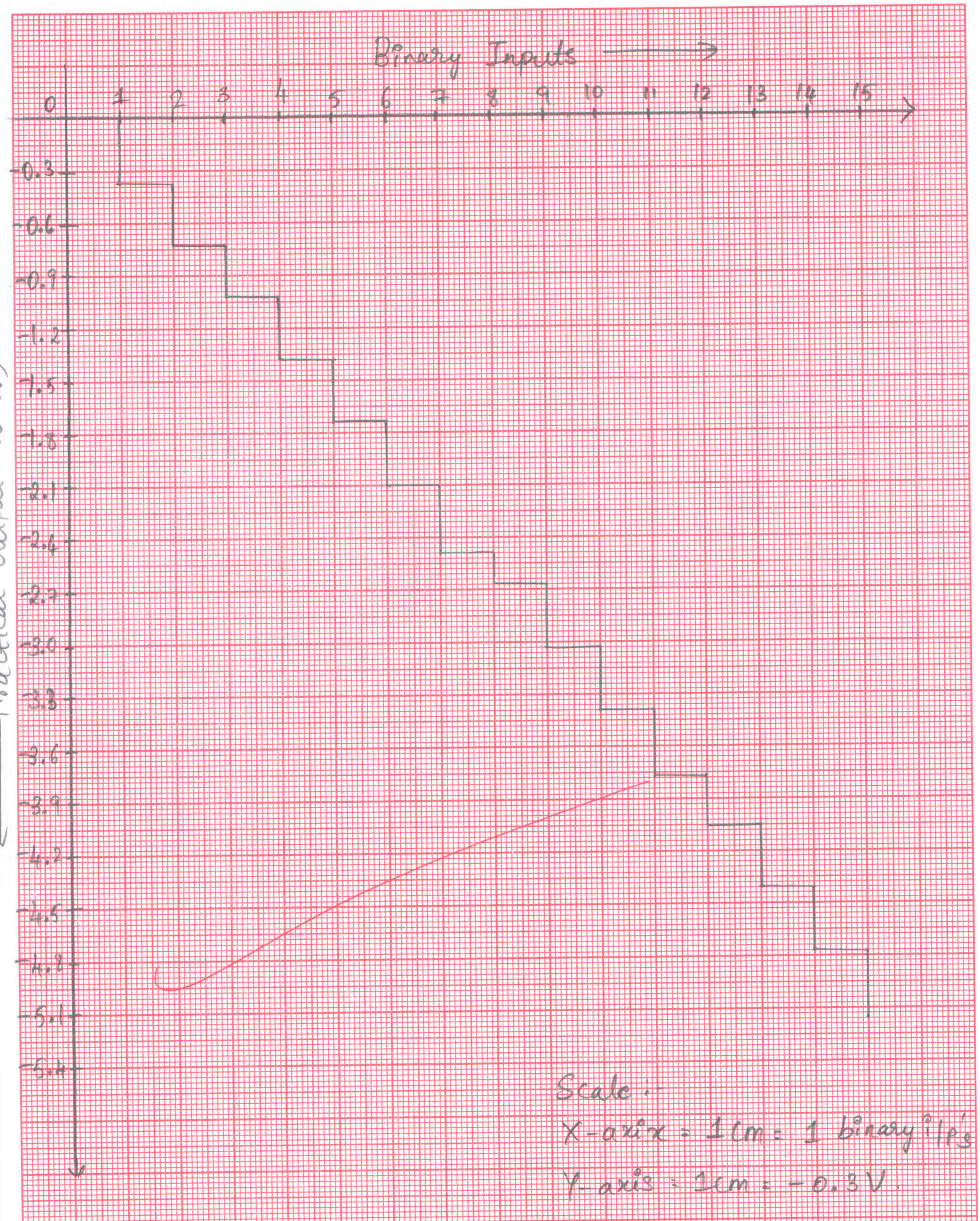
1. Connections are made as shown in the circuit diagram.
2. Apply binary inputs from 0000 to 1111 and note down the corresponding output voltage using multi-meter.
3. Compare these output voltage values with theoretical values.
4. Plot the graph of V_o (practical) verses binary inputs.

Tabulation.

Binary Inputs				Analog o/p voltage (V)	
B_3	B_2	B_1	B_0	Theoretical V_o	Practical V_o
0	0	0	0	0	0
0	0	0	1	-0.33	-0.376
0	0	1	0	-0.66	-0.72
0	0	1	1	-0.99	-1.07
0	1	0	0	-1.32	-1.38
0	1	0	1	-1.67	-1.76
0	1	1	0	-2	-2.10
0	1	1	1	-2.33	-2.48
1	0	0	0	-2.66	-2.67
1	0	0	1	-2.99	-3.04
1	0	1	0	-3.32	-3.39
1	0	1	1	-3.67	-3.76
1	1	0	0	-4	-4.05
1	1	0	1	-4.33	-4.43
1	1	1	0	-4.66	-4.77
1	1	1	1	-4.99(5V)	-5.15



Pin Details of IC74193



Scale :-

X-axis = 1 cm = 1 binary pulse

Y-axis = 1 cm = -0.3 V.

DATE 27/2/19

EXP. NO. 4

EXPT. TITLE : Digital to Analog Converter.

(b) Digital to analog Converter using MOD-16 counter.

Aim - To design & conduct a 4-bit R-2R op-amp digital to analog converter by generating digital inputs using MOD-16 Counter.

Components Requirement.

SI. No	Components	Quantity
1	Regulated Power supply ±15V	1
2	IC741	1
3	IC74193	1
4	Resistors:	
	1 kΩ	3
	2.2 kΩ	6
	3.3 kΩ	1
5	Bread board, Connecting Wires	1 set
6	Multi-meter	1
7	IC Trainer kit	1

IC 74193 Binary UP/DOWN Presettable Counter:

PIN Name	Description
P0 – P3	Parallel data inputs.
Q0 – Q3	Outputs.
MR	Master Reset (Clr) low.
Load	Asynchronous parallel load (Active high)

Use of 74193 as up Counter:

Truth Table.

Clock	Q_3	Q_2	Q_1	Q_0
⎍	0	0	0	0
⎍	0	0	0	1
⎍	0	0	1	0
⎍	0	0	1	1
⎍	0	1	0	0
⎍	0	1	0	1
⎍	0	1	1	0
⎍	0	1	1	1
⎍	1	0	0	0
⎍	1	0	0	1
⎍	1	0	1	0
⎍	1	0	1	1
⎍	1	1	0	0
⎍	1	1	0	1
⎍	1	1	1	0
⎍	1	1	1	1

DATE 27/2/19

EXP. NO. 4

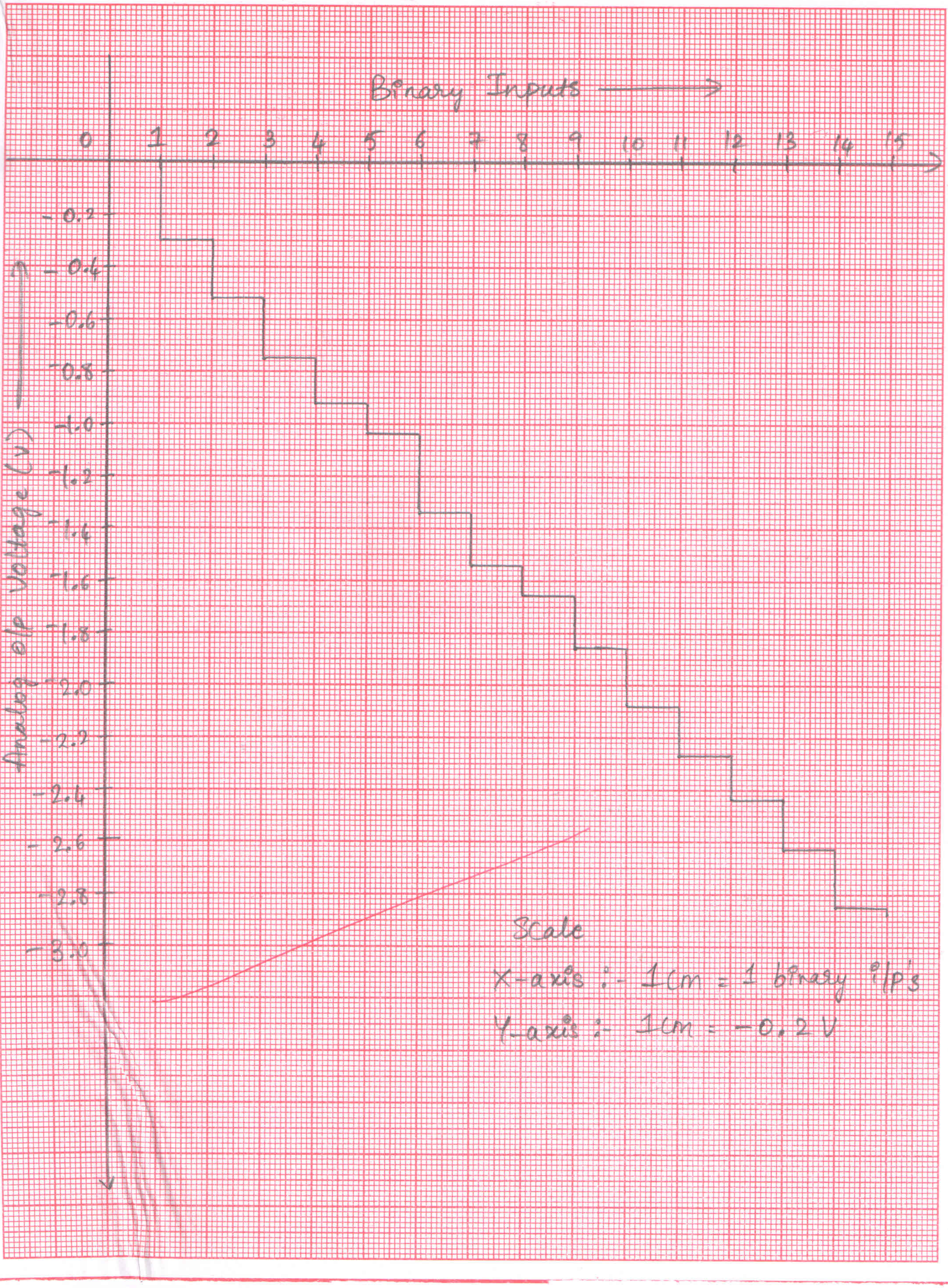
EXPT. TITLE : Digital to Analog Converter

Procedure

1. Connections are made as shown in the circuit diagram.
2. Apply binary inputs from 0000 to 1111 from the counter.
3. Measure the output voltage using multi-meter.
4. Plot the graph of V_o (practical) verses binary inputs.

Tabulation.

Binary Inputs B_3	B_2	B_1	B_0	Analog output Voltage Vo(V)
0	0	0	0	0
0	0	0	1	- 0.30
0	0	1	0	- 0.52
0	0	1	1	- 0.75
0	1	0	0	- 0.92
0	1	0	1	- 1.13
0	1	1	0	- 1.34
0	1	1	1	- 1.54
1	0	0	0	- 1.65
1	0	0	1	- 1.86
1	0	1	0	- 2.07
1	0	1	1	- 2.27
1	1	0	0	- 2.43
1	1	0	1	- 2.63
1	1	1	0	- 2.85
1	1	1	1	- 2.87


Binary Inputs
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
-1.4
-1.6
-1.8
-2.0
-2.2
-2.4
-2.6
-2.8
-3.0
Analog o/p voltage (V)
Scale
X-axis :- 1 cm = 1 binary i/p's
Y-axis :- 1 cm = -0.2 V

DATE 27/2/19

EXP. NO. 4

EXPT. TITLE : Digital to Analog Converter

Result :-

Full scale O/P Voltage	Theoretical Analog O/P Voltage (Full scale)	Practical analog O/P voltage using toggle switch (full scale)	Practical analog O/P voltage using MOD -16 Counter (Full scale)
5V	-4.99 V	-5.15 V	-2.87 V.

	Marks obtained
Record (10)	10
Observation (10)	10
Viva (5)	4
Total (25)	24

Saluva
6/3/19

Design :-

Let $I_c = 2mA$, $V_{CE} = 3V$.

$\beta = 100$ & $V_{RE} = 2V$ for BF 194 / SL 100.

$$R_E = V_E / I_E = \frac{V_{RE}}{I_C} = \frac{2V}{2mA} = 1k\Omega.$$

Because $I_E = I_C$.

$R_E = 1K\Omega$.

$V_{CC} = I_C R_C + V_{CE} + V_{RE}$

Therefore, $I_C R_C = V_{CC} - V_{CE} - V_{RE}$.

$= 6 - 3 - 2$

$= 1V$.

$$R_C = \frac{1}{I_C} = \frac{1}{2 \times 10^{-3}} = 500\Omega = 470 \text{ (std value)}.$$

For transistor to be in cut off region.

$\frac{R_2}{R_1} = \frac{1}{20}$. Therefore, $R_1 = 20 R_2$.

Choose, $R_2 = 2.2 k\Omega$.

Therefore, $R_1 = 44K\Omega$ Choose $R_1 = 47k\Omega$.

DATE 6/3/19

EXP. NO. 5

EXPT. TITLE : BJT Mixer UP/DOWN Conversion

Aim :-

To design a transistor mixer circuit using BJT and demonstrate the mixing action (up & Docon conversion) for an IFT of 455 kHz.

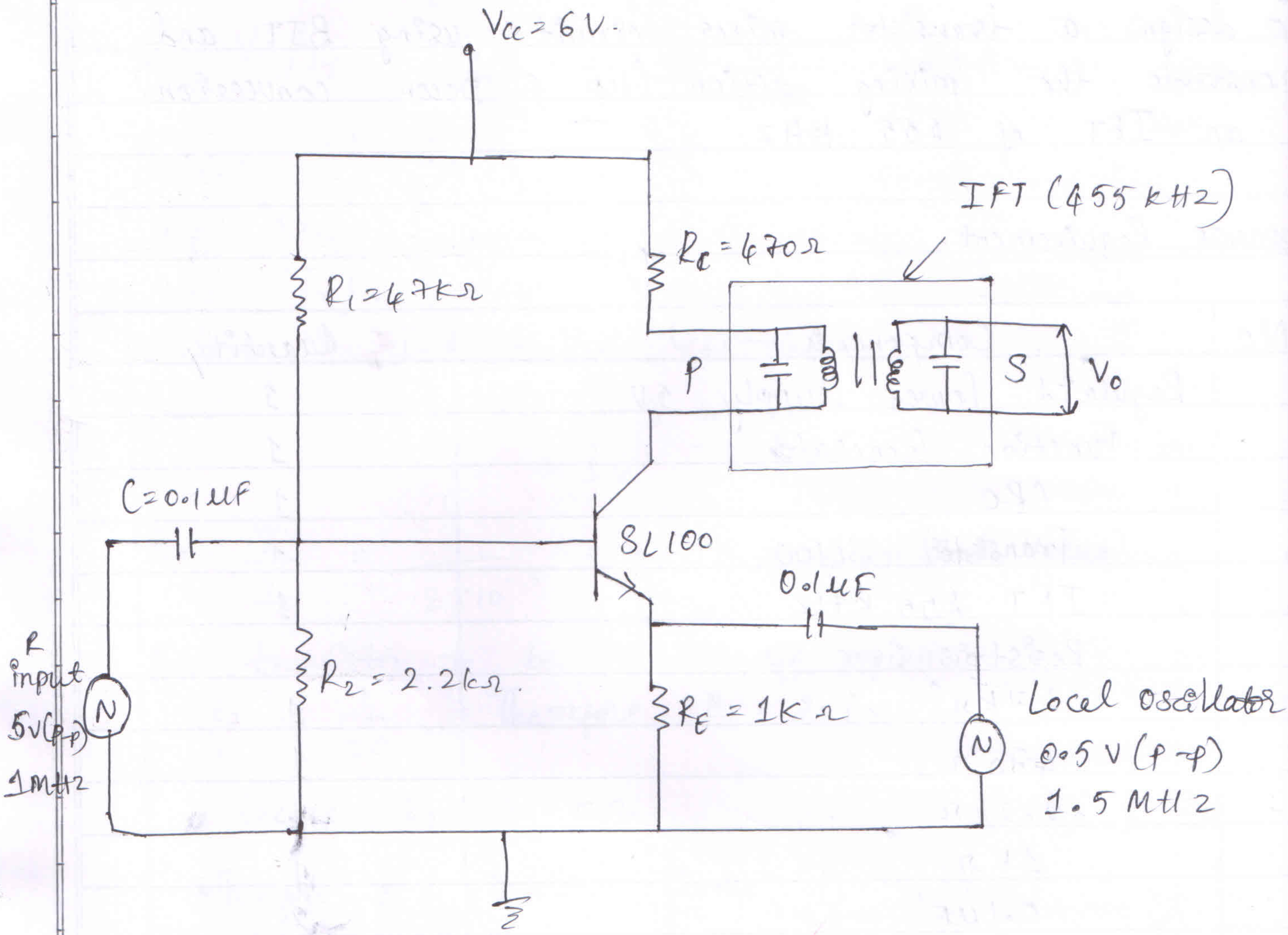
Components Requirement.

Sl. No	Components	Quantity
1.	Regulated Power supply 5V	1
2.	Function Generator	1
3.	CRO	1
4.	Transistor SL100	1
5.	IFT 455 KHz	1
6.	Resistors :	
	47kΩ	1
	470Ω	1
	2.2kΩ.	1
	1kΩ	1
	0.1μF	2
7	Bread board, Connecting Wires	1 set

Theory :-

Transistor mixer is also known as RF amplifier. RF amplifier provides initial gain & selectivity. Figure shows the RF amplifier circuits. It is a tuned circuit followed by an amplifier. The RF amplifier is usually a simple class. A typical bipolar circuit is shown in fig.

Transistor Mixer (up/down Conservation)



DATE 6/3/19

EXP. NO. 5

EXPT. TITLE : BJT Mixer UP/Down Conversion

The values of resistors R_1 and R_2 in the bi-polar circuit are adjusted such that the amplifier works as class A amplifier. The RF (input antenna) is connected through coupling capacitor (C_1) to the base of the transistor. This makes the circuit very broad band, as the transistor will amplify virtually any signal picked up by the RF input (Antenna). However the collector is tuned with a parallel resonant circuit to provide the initial selectivity for the mixer input. And also local oscillator input is connected through coupling capacitor to the emitter of the transmitter.

D° Procedure

1. Before wiring the circuit check all the components using multi-meter.

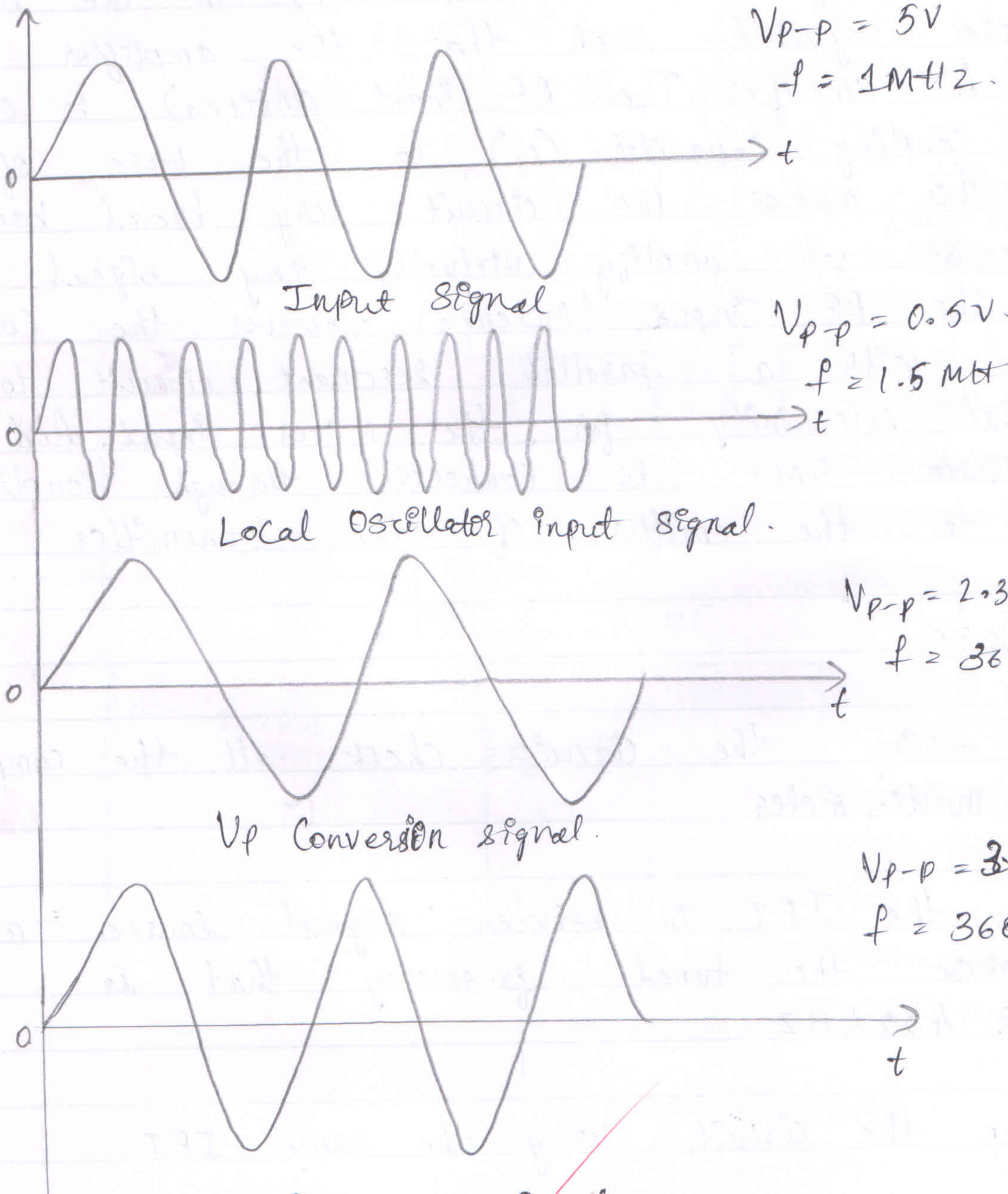
2. Connect the IFT in between signal source and CRO. Measure the tuned frequency that is $f_{IFF} = 455$ kHz.

3. Plug up the circuit using the same IFT.

4. Switch ON the signal source V_1 & V_2 (use always MHz frequency range). Adjust V_2 amplitude to be 10 times larger than V_1.

5. For Ex: $V_1 = 5V(p-p)$ & $V_2 = 0.5V(p-p)$.

BJT Mixer Wave forms



$V_{p-p} = 5V$
$f = 1MHz$.

Input Signal

$V_{p-p} = 0.5V$.
$f = 1.5 MHz$.

Local Oscillator input signal.

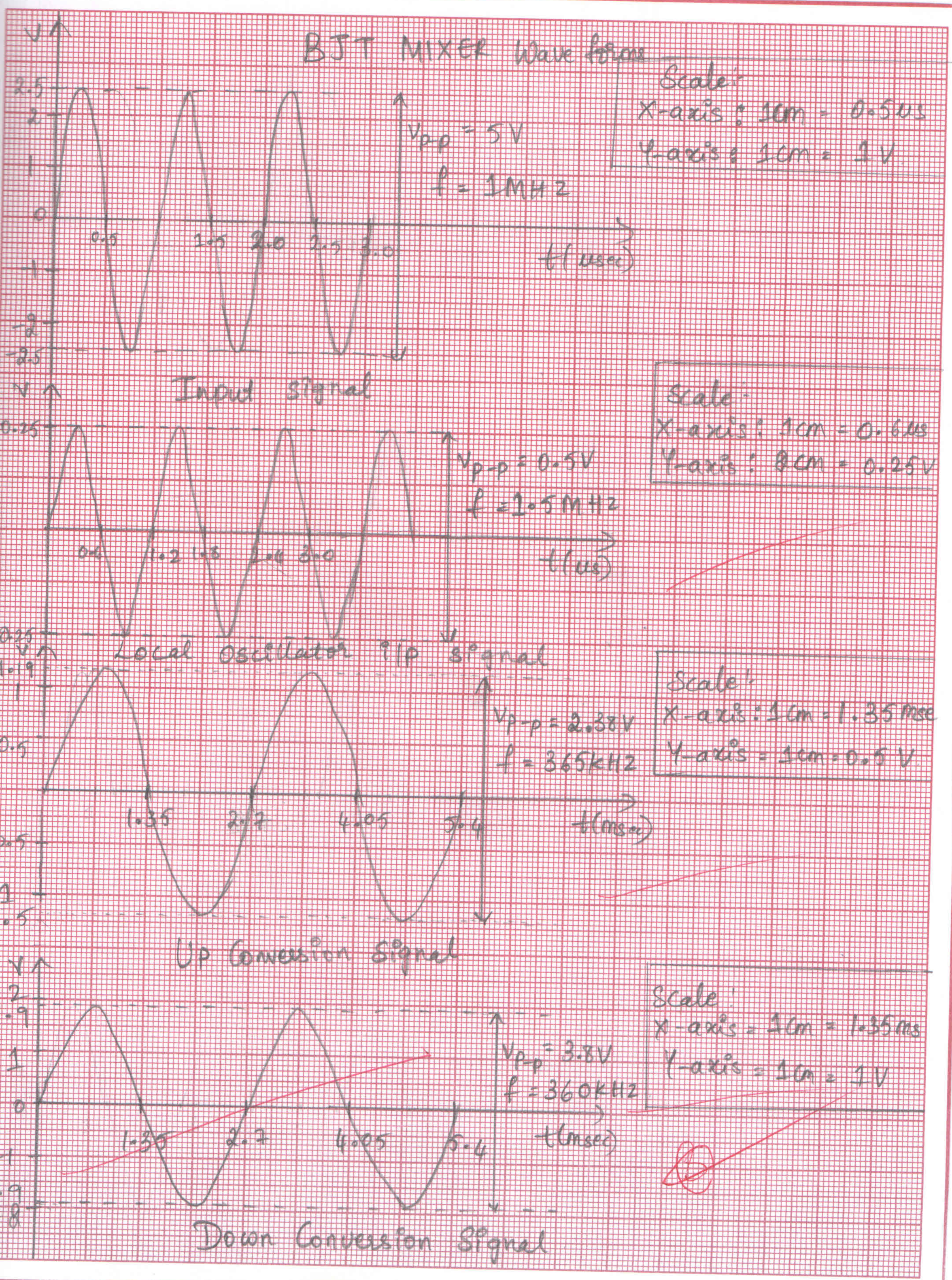
$V_{p-p} = 2.38V$.
$f = 365 kHz$.

Vp Conversion signal.

$V_{p-p} = 3.8V$.
$f = 360 kHz$.

Down Conversion signal.

BJT MIXER Waveforms



6. Vary the frequency of RF source V_1 & local oscillator source V_2 such that we can see undistorted & sine wave on CRO.

7. Note down V_1 & V_2 the difference should be equal to IFT frequency = 455 KHz.

8. For up conversion $f_{osc} > f_{RF}$ & for down conversion $f_{RF} > f_{osc}$.

9. Verify the same & tabulate readings in tabular column.

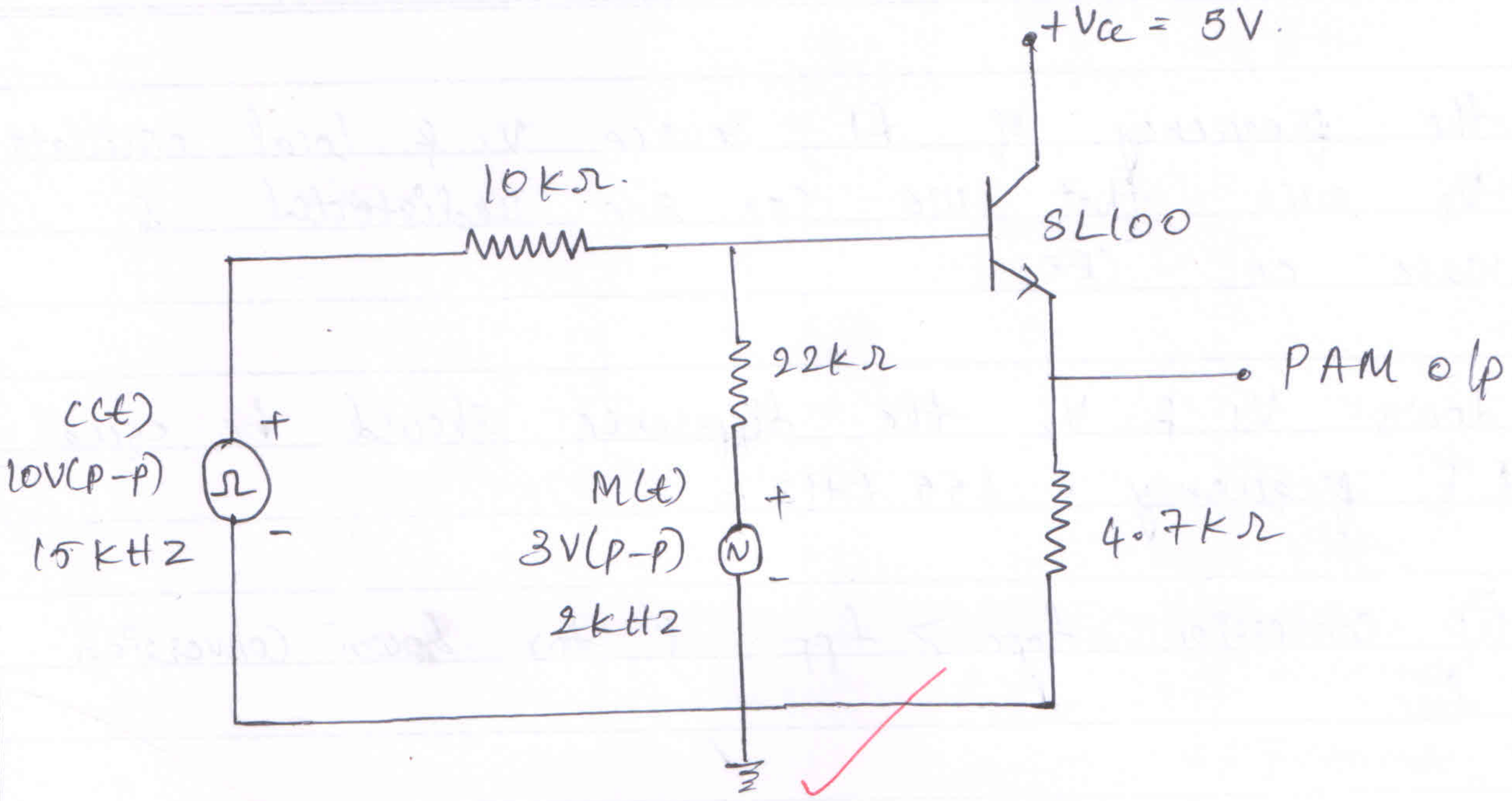
Result :-

(a) For up conversion, $f_{osc} = 1.365$ MHz, $f_{RF} = 1$ MHz
$V_{p-p} = 2.38$ V & F = 365 KHz.
Difference in frequencies, f = 365 KHz.

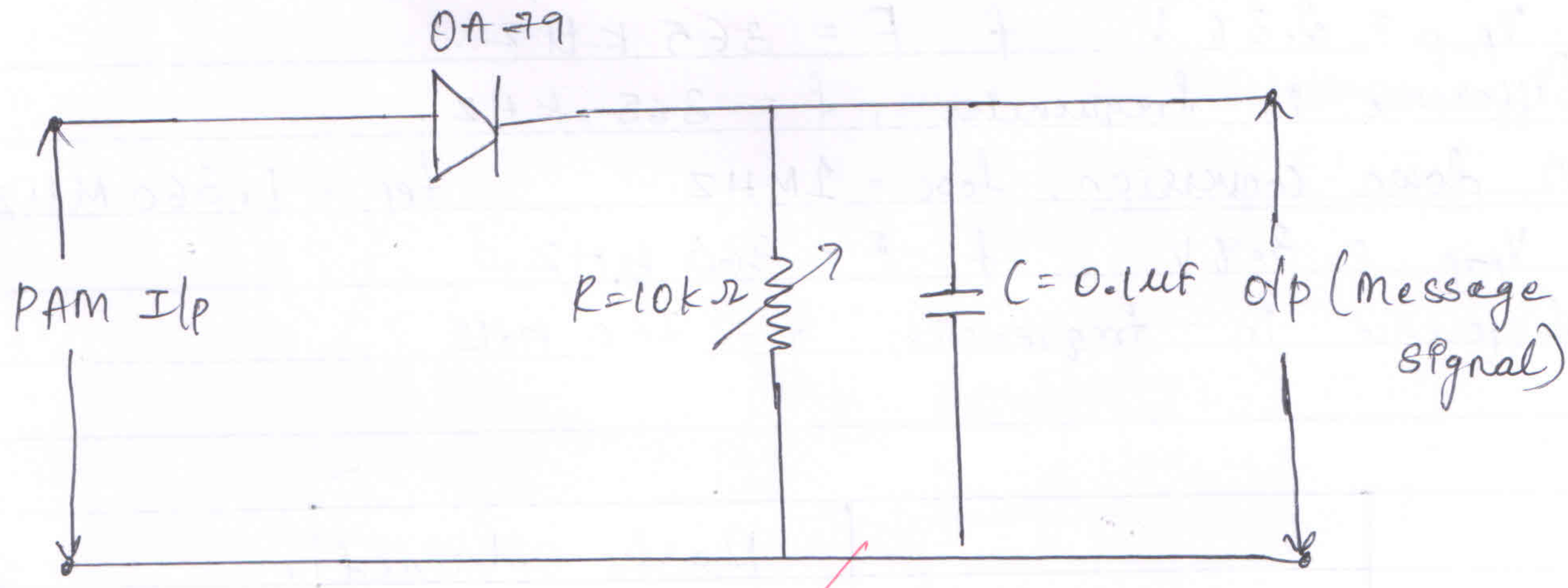
(b) For down conversion, $f_{osc} = 1$ MHz $f_{RF} = 1.360$ MHz,
$V_{p-p} = 3.8$ V & F = 360 KHz.
Difference in frequencies, f = 360 KHz.

	Marks Obtained
Observation (10)	10
Record (10)	10
Viva (5)	3
Total (25)	23

Pulse Amplitude Modulation (PAM)



Demodulation Circuit for PAM.



DATE 20/3/19 | EXPT. TITLE : Generation & detection of Pulse sampling (PAM) & Flat top sampling. | PAGE NO. 25

EXP. NO. 6

Aim :-

To demonstrate an experiment to generate a pulse sampled signal and its reconstruction.

Components required :-

SI. NO	Components	Quantity
1	Regulated Power supply 5V.	1
2	Function Generator	1
3	CRO	1
4	Transistor SL100	1
5	Resistors:	
	10 kΩ	1
	22 kΩ	1
	4.7 kΩ	1
	10 kΩ Pot	1
	0.1 μF	1
6	OA79 Diode.	1
7	Bread board, Connecting Wire.	1

Theory :-

In pulse amplitude modulation (PAM) the amplitude of the pulses are varied in accordance with the modulating signal denoting the modulating signal as m(t) signal. The balanced mixer / modulators are frequency used as multipliers for this purpose. The o/p is a series of pulses, the amplitudes of which vary in proportion

to the modulating signal.

The particular form of amplitude modulation is referred to as natural PAM because the tops of the pulses follow the shape of the modulating signal.

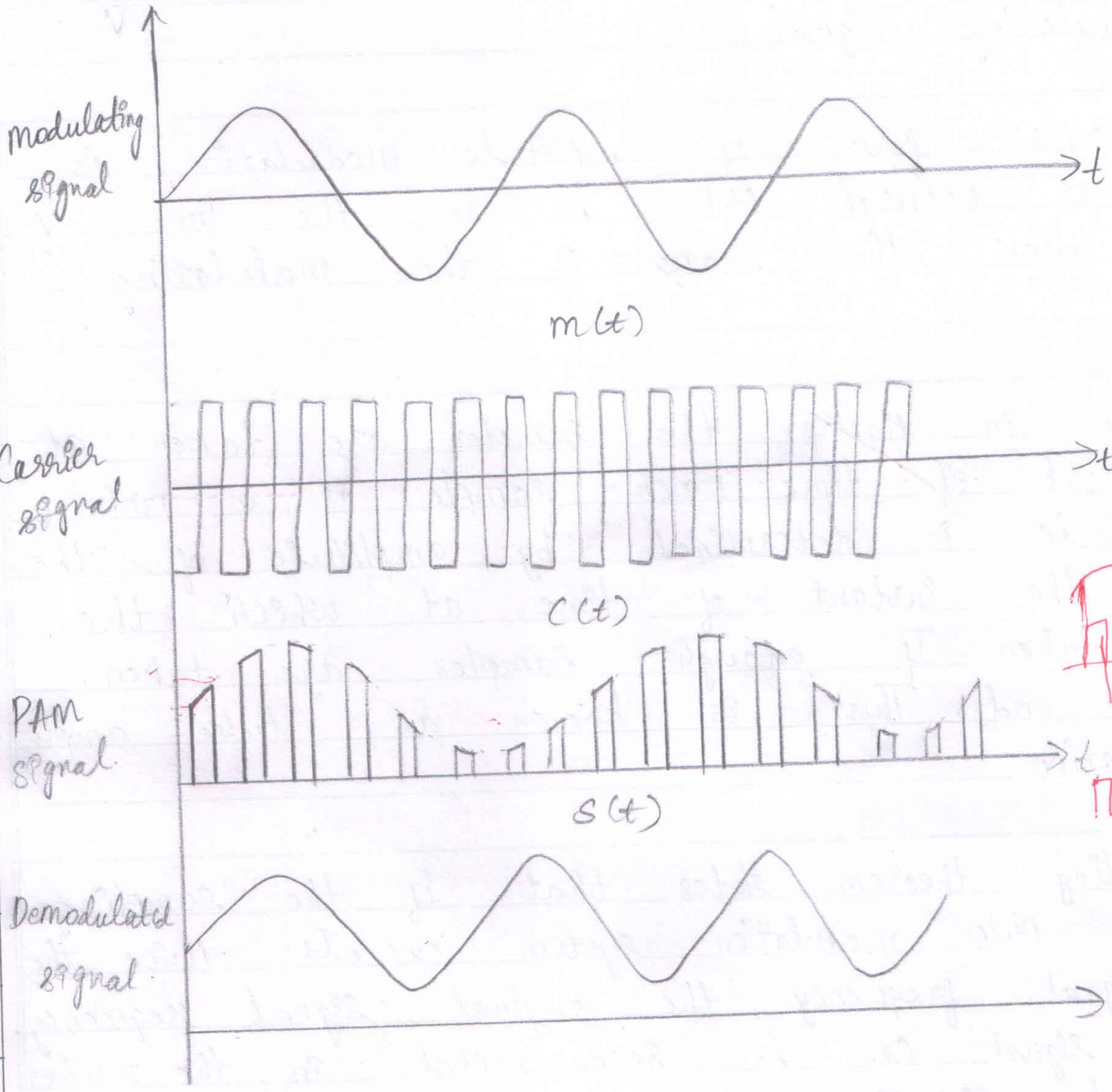
As shown in figure the samples are taken at regular interval of time. Each sample is a pulse, whose amplitude is determined by amplitude of the variable at the instant of time at which the sample is taken. If enough samples are taken, the receiving end. This is known as "Pulse amplitude modulation.

The sampling theorem states that, if the sampling rate in any pulse modulation system exceeds twice the maximum signal frequency, the original signal frequency, the original signal can be reconstructed in the receiver with minimal distortion.

Procedure :-

1. Make the connections as shown in circuit diagram.
2. Set the carrier amplitude to around 10V (p-p) and frequency in the range of 5 kHz to 15 kHz.
3. Set the signal amplitude to around 3V (p-p) and frequency to 2kHz.

PULSE SAMPLING WAVEFORMS.







Observations.

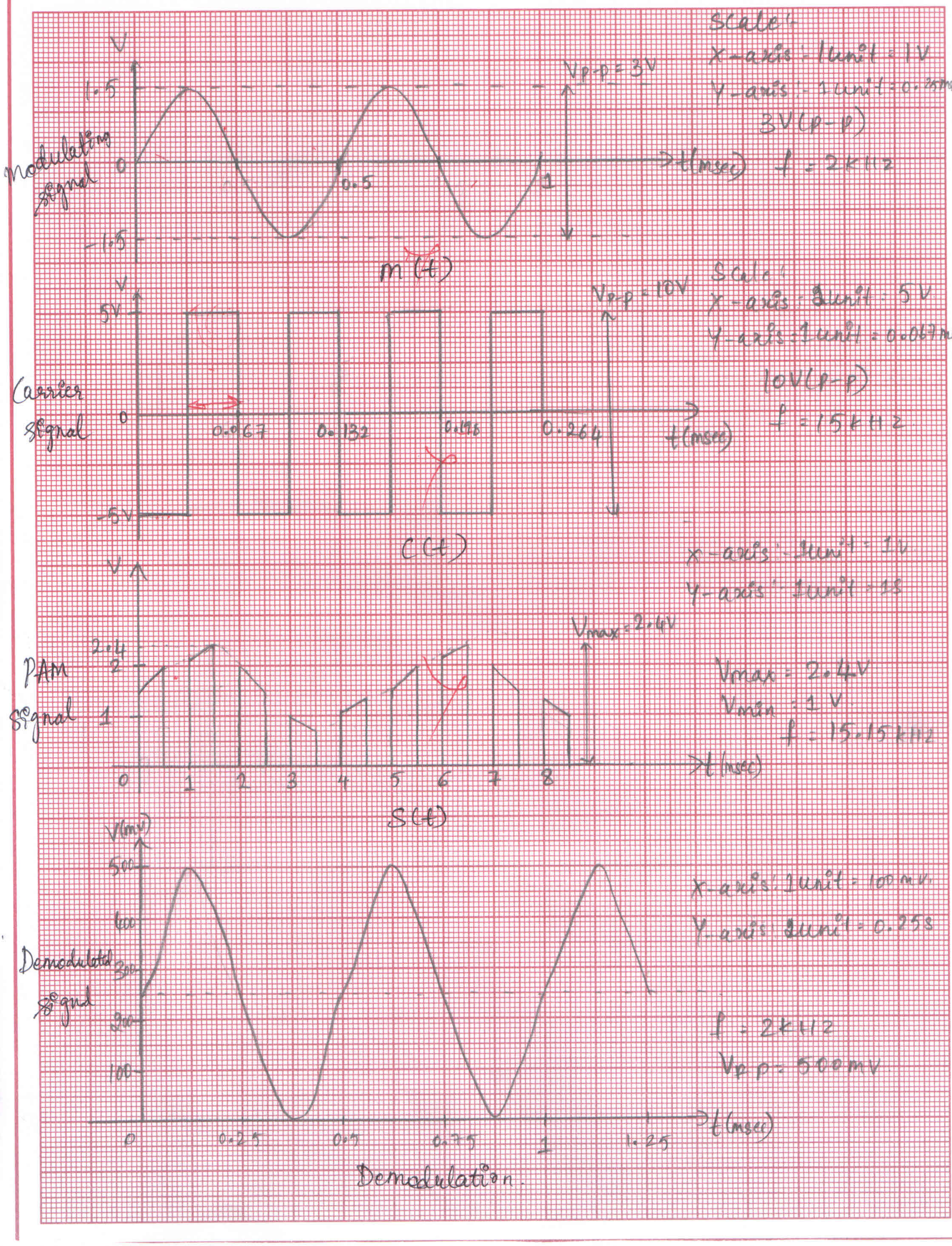
Output voltage Flat top sampled signal.

$V_{max} = 2.4\ V$

$V_{min} = 1\ V$.

Demodulated signal.

$V_0 = \underline{500}\ mV$ at $f = \underline{2\ kHz}$


V
1.5
0
-1.5
Modulating signal
0.5
1
t(msec)
Vp-p = 3V
m(t)
Scale:
X-axis: 1 unit = 1 V
Y-axis: 1 unit = 0.25 msec.
3V(p-p)
f = 2KHz
V
5V
0
-5V
Carrier signal
0.067
0.132
0.198
0.264
t(msec)
C(t)
Vp-p = 10V
Scale:
X-axis: 1 unit = 5 V
Y-axis: 1 unit = 0.067 msec
10V(p-p)
f = 15 KHz
V
2.4
2
1
PAM signal
0
1
2
3
4
5
6
7
8
t(msec)
S(t)
Vmax = 2.4V
X-axis: 1 unit = 1V
Y-axis: 1 unit = 1s
Vmax = 2.4V
Vmin = 1 V
f = 15.15 KHz
V(mV)
500
400
300
100
Demodulated signal
0
0.25
0.5
0.75
1
1.25
t(msec)
X-axis: 1 unit = 100 mV
Y-axis: 1 unit = 0.25s
f = 2KHz
Vp-p = 500mV
Demodulation.

4. Connect the CRO at the emitter of the transistor and observe the PAM waveform.

5. Now to verify sampling theorem, keep the modulating signal frequency to say 2kHz and the carrier frequency to twice that of modulating signal frequency and observe the output waveform. Connect this output to the demodulator circuit and observe the signal if it matches with the signal then sampling theorem is verified.

6. Check the demodulated output for different frequencies of carrier wave.

7. Plot the waveforms.

(b) Flat top sampling.

Aim :-

To demonstrate an experiment to generate a flat top sampled signal and its reconstruction.

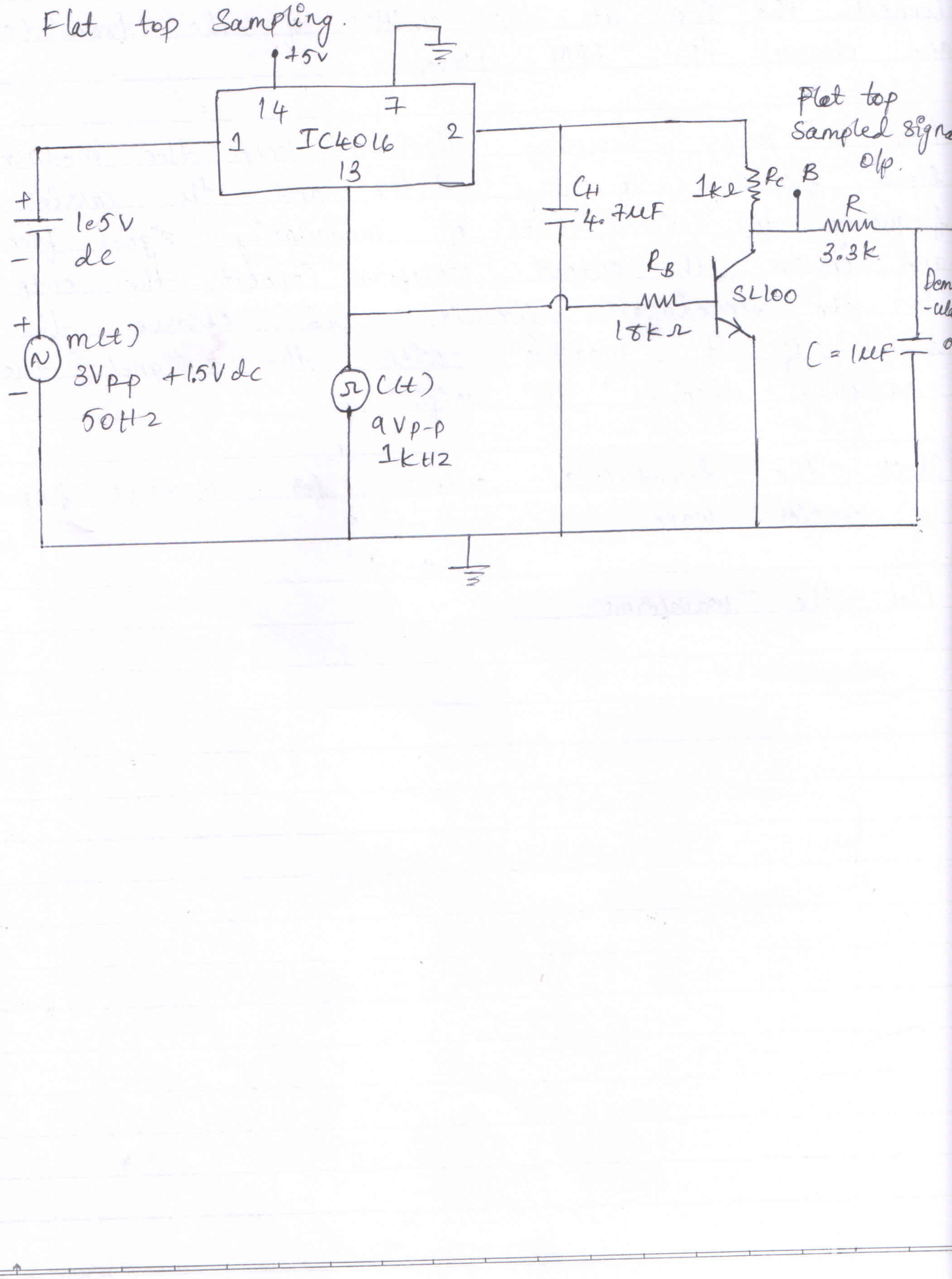
Components Requirement.

SI. NO	Components	Quantity
1.	Regulated Power Supply 5V	1
2.	Function Generator	1
3.	CRO	1
4.	IC 4016	1
5	SL100	1
6	Resistors :	
	18 kΩ	1
	1 kΩ	1
	3.3 kΩ.	1
	4.7 μF	1
	1 μF	1
7.	Bread board, Connecting Wires	1 Set

Theory :-

During transmission noise is introduced at the top of the transmission pulse which can be easily removed if the pulse is in the form of flat top here top of the samples are flat. That is they have constant amplitude. Flat top sampling makes use of sampled and hold

Flat top Sampling.



Flat top Sampled signal o/p.

circuit for the generation of flat top sampling can be mathematically considers as convolution of the sampled signal and the pulse signal. It is mostly used in digital transmission, the top of the slice does not preserve the shape of the waveform.

Procedure :-

1. Connections are made as shown in the circuit diagram.

2. Set the sinusoidal modulating signal for amplitude of about 3V peak to peak at 50Hz signal and apply DC voltage of 1.5V to the input of the circuit simultaneously.

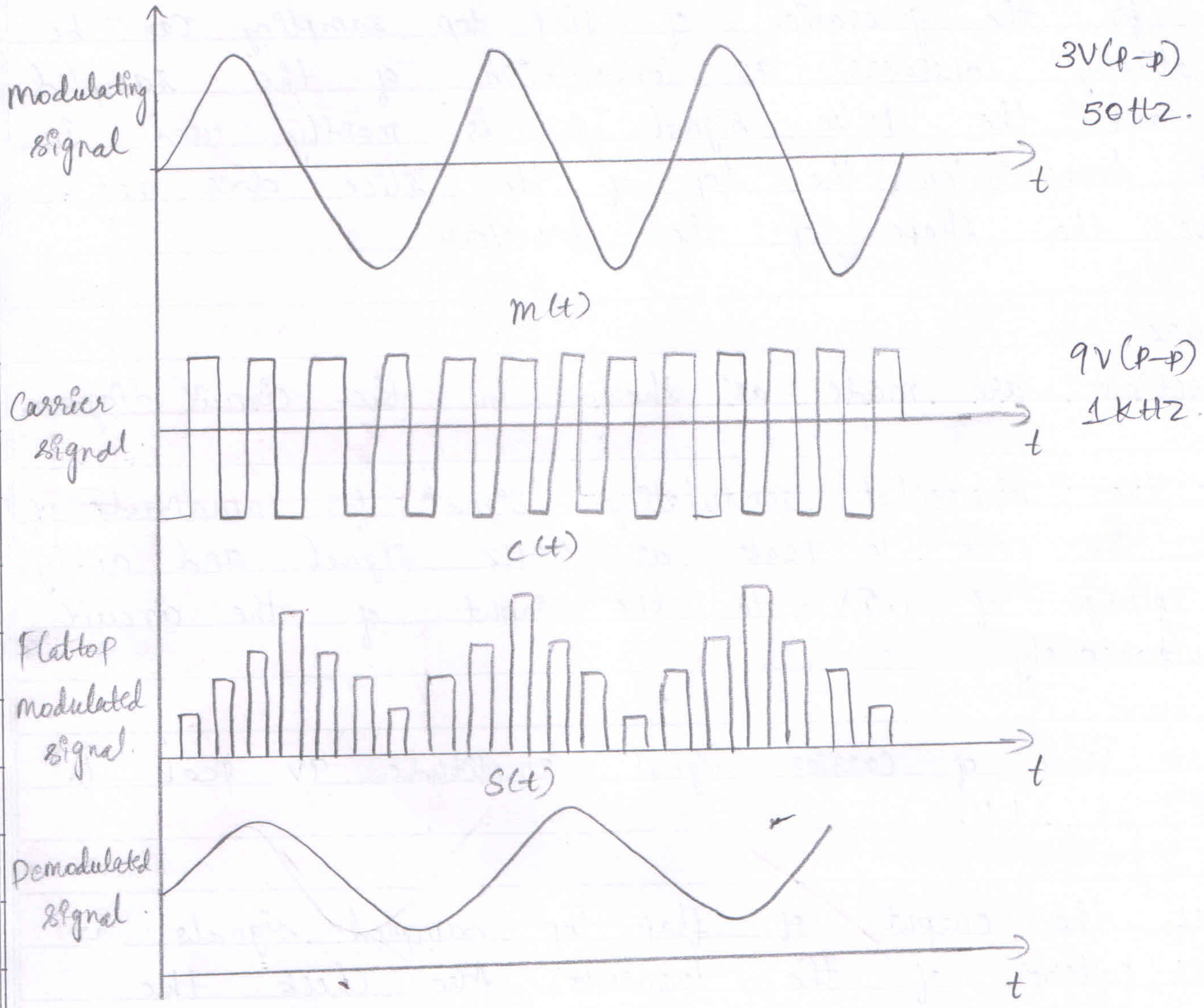
3. Square wave of carrier signal amplitude 9V peak to peak at 1KHz.

4. Check the output of flap top sampled signals at the collector of the transistor. Also check the demodulated output across the capacitor.

5. Calculate the amplitude (V_{max} and V_{min}) and frequency of modulated signal.

6. Calculate the amplitude and frequency of demodulated signal.

Flat top Sampling waveforms.



Observations.

Output Voltage V_o Flat top Sampled signal.

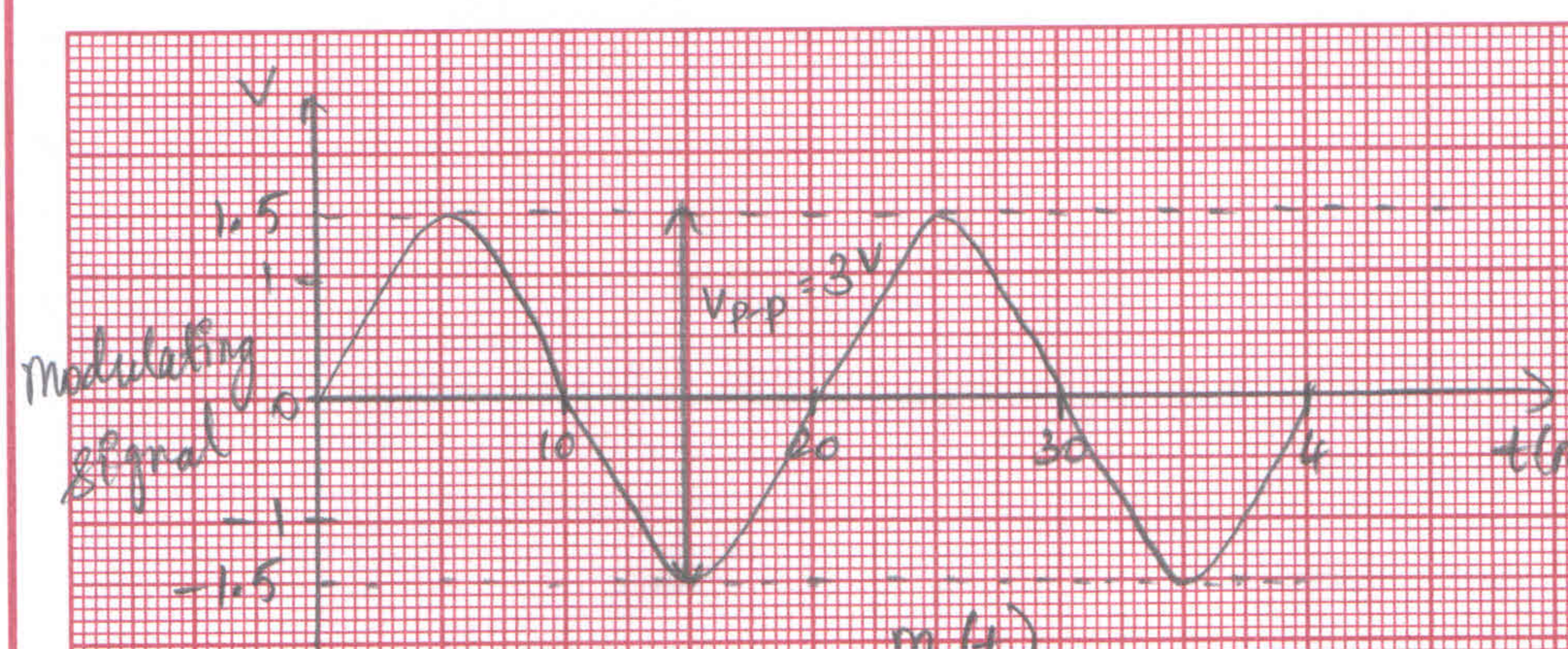
$V_{max} = 1.7V$

$V_{min} = 0.7V$

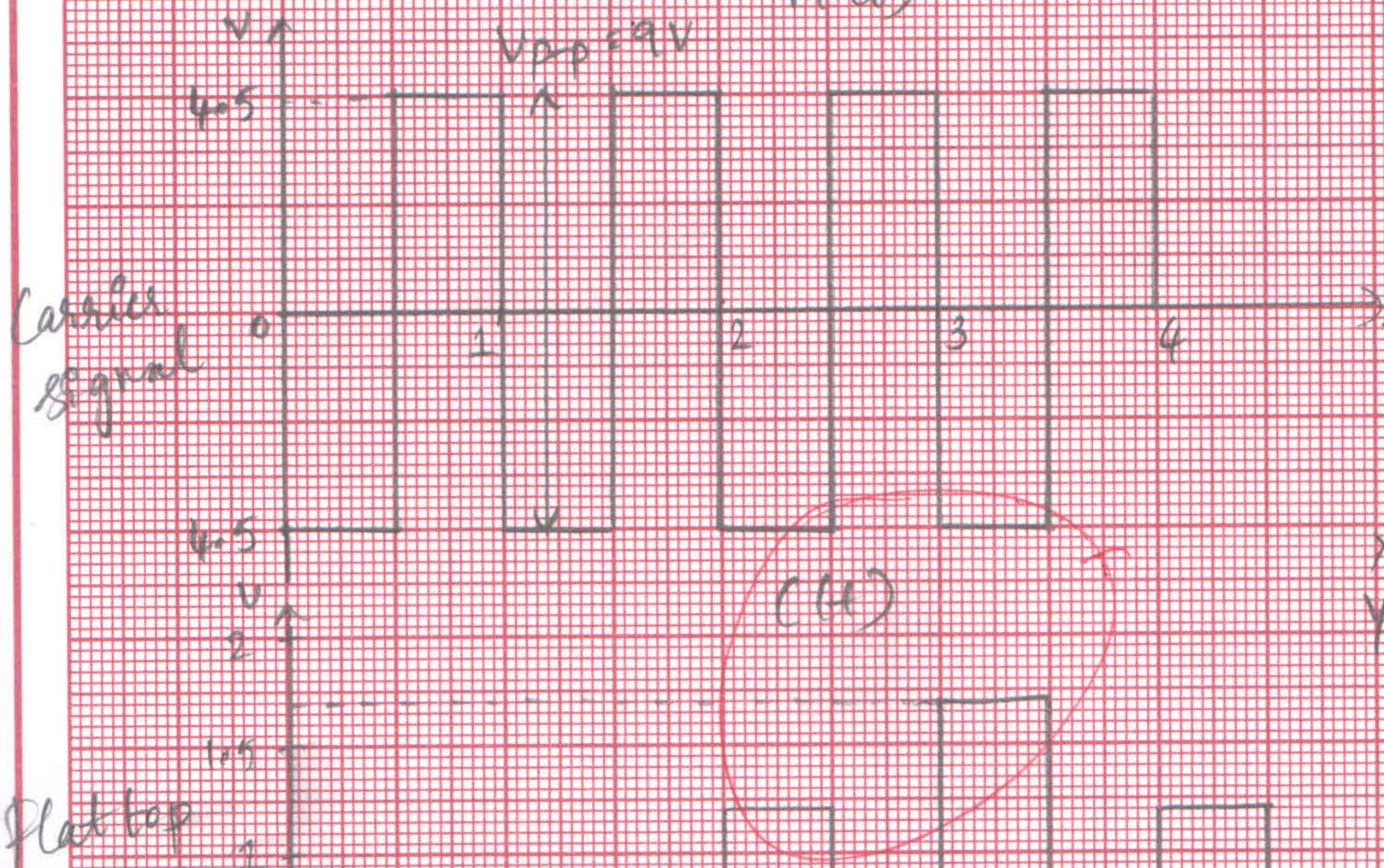
Demodulated signal.

$V_o =$ 530V(p-p) at $f =$ 50.5Hz.

Scale:
X-axis - 1 unit = 1 V
Y-axis - 2 unit = 10 msec
f = 50 Hz
3V (P-P)



Scale:
X-axis - 2 units = 4.5 V
Y-axis - 2 units = 1 msec
9V (P-P)
f = 1 kHz



X-axis: 1 unit = 0.5 V
Y-axis: 1 unit = 1 sec
Vmax = 1.7 V
Vmin = 0.7 V
f = 1 kHz

X-axis = 1 unit = 100 V
Y-axis = 4 units = 0.01 s
Vp-p = 530 V.
f = 50.5 Hz

Demodulation

Result :-

(a) Pulse sampled signal is generated and demodulated

(b) Flat top sampled signal is generated and demodulated

	Marks obtained.
Observation (10)	09
Record (10)	09
Viva (5)	04
Total (25)	22

DATE 3/4/19 | EXPT. TITLE : Astable and Monostable multivibrator | PAGE NO. 31

EXP. NO. 7

Aim :-

To design and conduct an experiment using IC555 timer
(a) Astable Multivibrator for given duty cycle.
(b) Monostable multivibrator for a given pulse width.

(a) Astable multivibrator.

Components required

Sl. No.	Components	Quantity
1.	Regulated Power supply 5V.	1
2.	Function Generator.	1
3.	CRO.	1
4.	IC555.	1
5.	Resistors:	
	3.3 kΩ.	2
	2.2 kΩ.	1
	4.7 kΩ.	1
	1 kΩ.	1
	1 μF, 0.01 μF, 0.001 μF, 0.1 μF	4
	IN4007 Diode	1
6.	Bread board, Connecting Wires	1 set

Theory :-

An astable multivibrator is a circuit that is continuously switching its output voltage between high and low levels.

(a) Astable Multivibrator

Design :-

$$T_{high} = 0.69 R_A C.$$

$$T_{low} = 0.69 R_B C.$$

$$\text{Duty cycle} = D = \frac{t_{High}}{T} = \frac{R_A}{R_A + R_B}$$

$$\text{Frequency}, f = \frac{1}{T}$$

(i) Duty cycle less than 50% (36%)

Frequency = 200 Hz. $T = 5ms$.

$$D = \frac{t_{high}}{T}$$

Therefore, $T_{high} = T \times D = 5ms \times 0.36 = 1.8 ms.$

$$T_{high} = 0.69 R_A C$$

Let $C = 1\mu F$.

Therefore, $R_A = 2.6 K\Omega$ (Use $2.2 K\Omega$) std value.

$T_{low} = T - T_{high} = 5ms - 1.8ms = 3.2 ms$

$T_{low} = 0.69 R_B C.$

Therefore, $R_B = 4.64 K\Omega$ Use $4.7 K\Omega$ std. value.

(ii) Duty cycle more than 50% (64%)

Frequency = 200+12.

$$T = \frac{1}{f} = \frac{1}{200} = 5 msec.$$

$D = 0.64$, let $C = 1\mu F$.

$$D = \frac{t_{High}}{T}$$

$t_{high} = D \times T = 0.64 \times 5ms = 3.2 msec.$

$t_{high} = 0.69 \times R_A C$

$R_A = \frac{t_{high}}{0.69 \times C} = \frac{3.2 msec.}{0.69 \times 10^{-6}} = 4.6 k\Omega$ (Select $4.7 k\Omega$)

$t_{low} = T - t_{high} = 5m - 3.2m = 1.8 msec.$

$t_{low} = 0.69 R_B C$

$R_B = \frac{1.8 ms}{0.69 \times 10^{-6}} = 2.6 k\Omega$ (Select $2.2 k\Omega$).

(iii) Duty cycle equal to 50%.

Frequency = 200 Hz.

$T = \frac{1}{f} = \frac{1}{200} = 5 msec.$

$D = \frac{t_{high}}{T} = \frac{R_A}{R_A + R_B}$

$t_{high} = 0.69 R_A C \qquad t_{low} = 0.69 R_B C.$

$D = 0.5$

$T = t_{high} + t_{low}$

$t_{high} = 0.69 R_A C$

$t_{high} = D \times T = 0.5 \times 5 ms = 2.5 msec.$

$t_{low} = T - t_{high} = 5m - 2.5m = 2.5 msec.$

$t_{high} = 0.69 R_A C.$

$R_A = \frac{t_{high}}{0.6 \times C} = \frac{2.5 msec}{0.69 \times 10^{-6}} = 3.3 k\Omega.$

$R_A = R_B = 3.3 k\Omega.$

DATE 3/4/19
EXP. NO. 7
EXPT. TITLE : Astable and Monostable multivibrator

It has no stable state. An astable multivibrator using an operational amplifier is done when the circuit output is at the positive saturation level, current flows into the capacitor, charging it positive at the top. The output then rapidly switches to the op-amp negative saturation level. Now current flows from the capacitor removing its positive charge and recharging it with the opposite polarity. Then the recharging it with the opposite polarity. Then the op-amp output rapidly switches back to the positive saturation level and the cycle starts again.

It is seen that the circuit is a square wave generator with an output that swings between the op-amp positive and negative saturation levels.

Procedure.

1. Connect the circuit as per the circuit diagram.

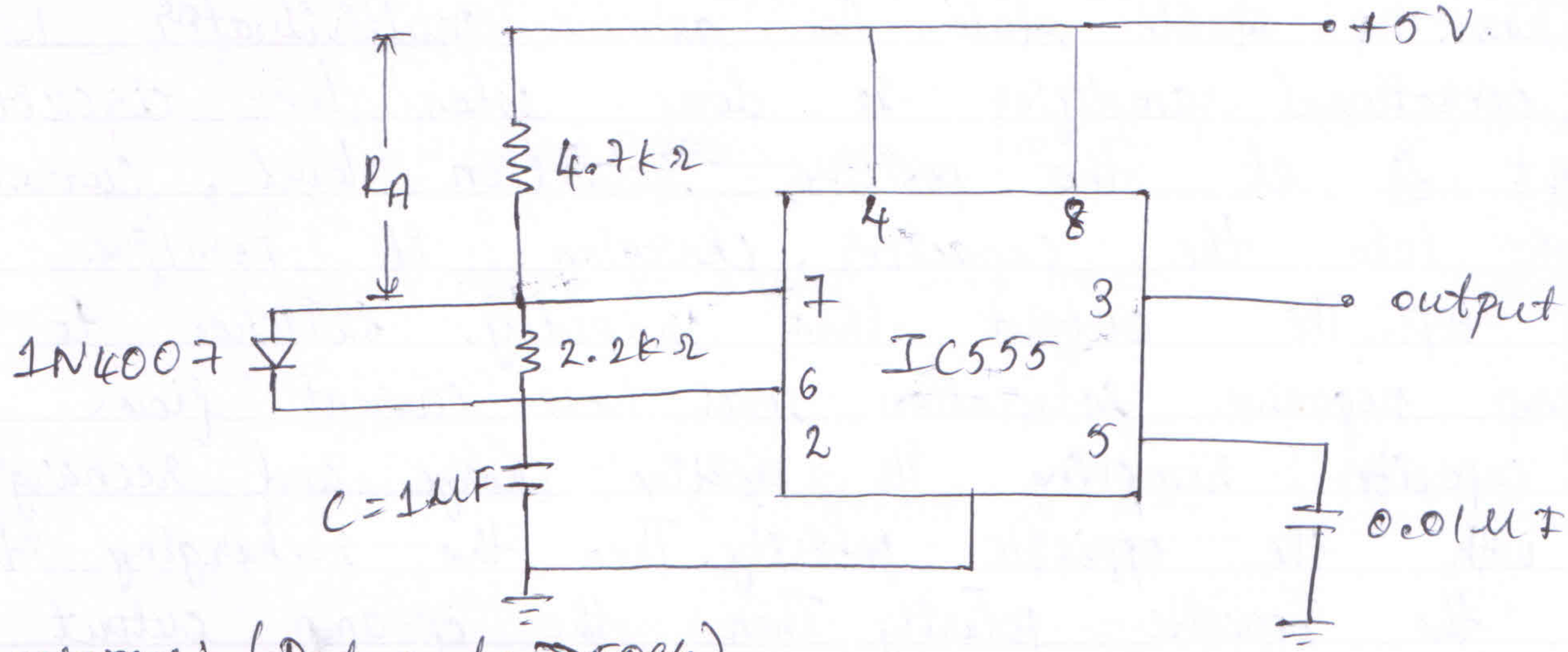
2. Switch on the supply and note down the output waveform at pin no. 3 on the CRO.

3. Note, T_{high} = ___, T_{low} = ___ & V_{pp} = ___.

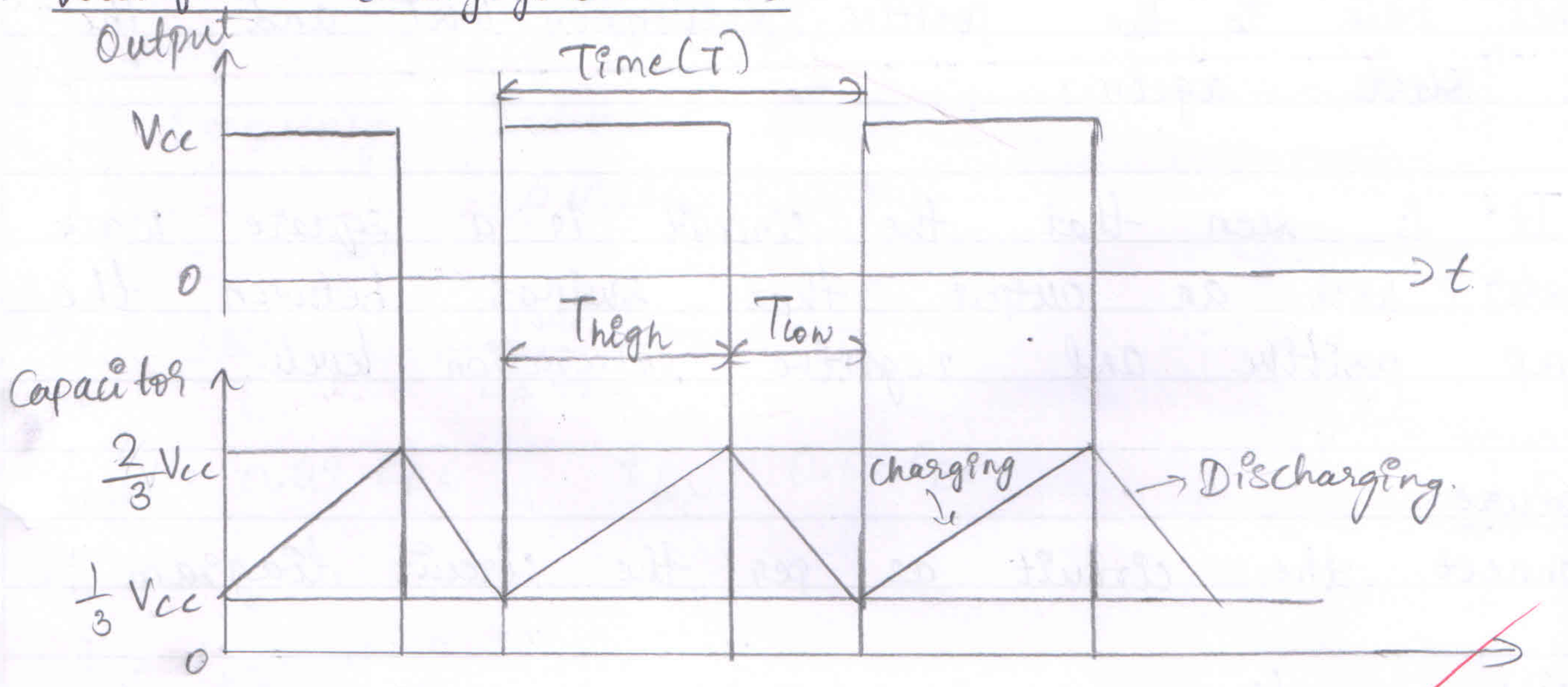
4. Compare theoretical and practical time periods.

5. Draw the input and output waveforms for different duty cycles.

Astable Multivibrator.



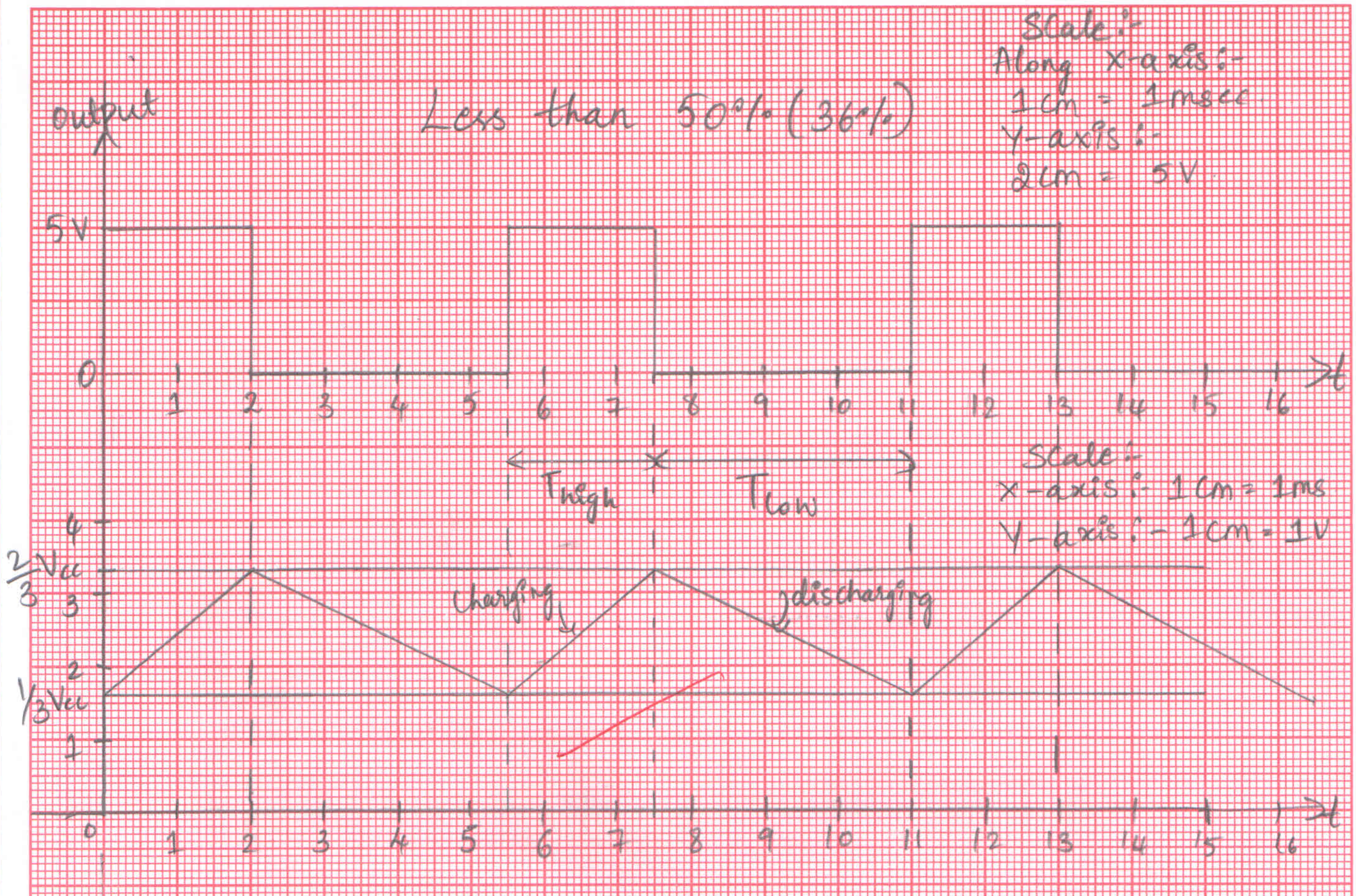
Waveforms :- (Dutycycle > 50%)



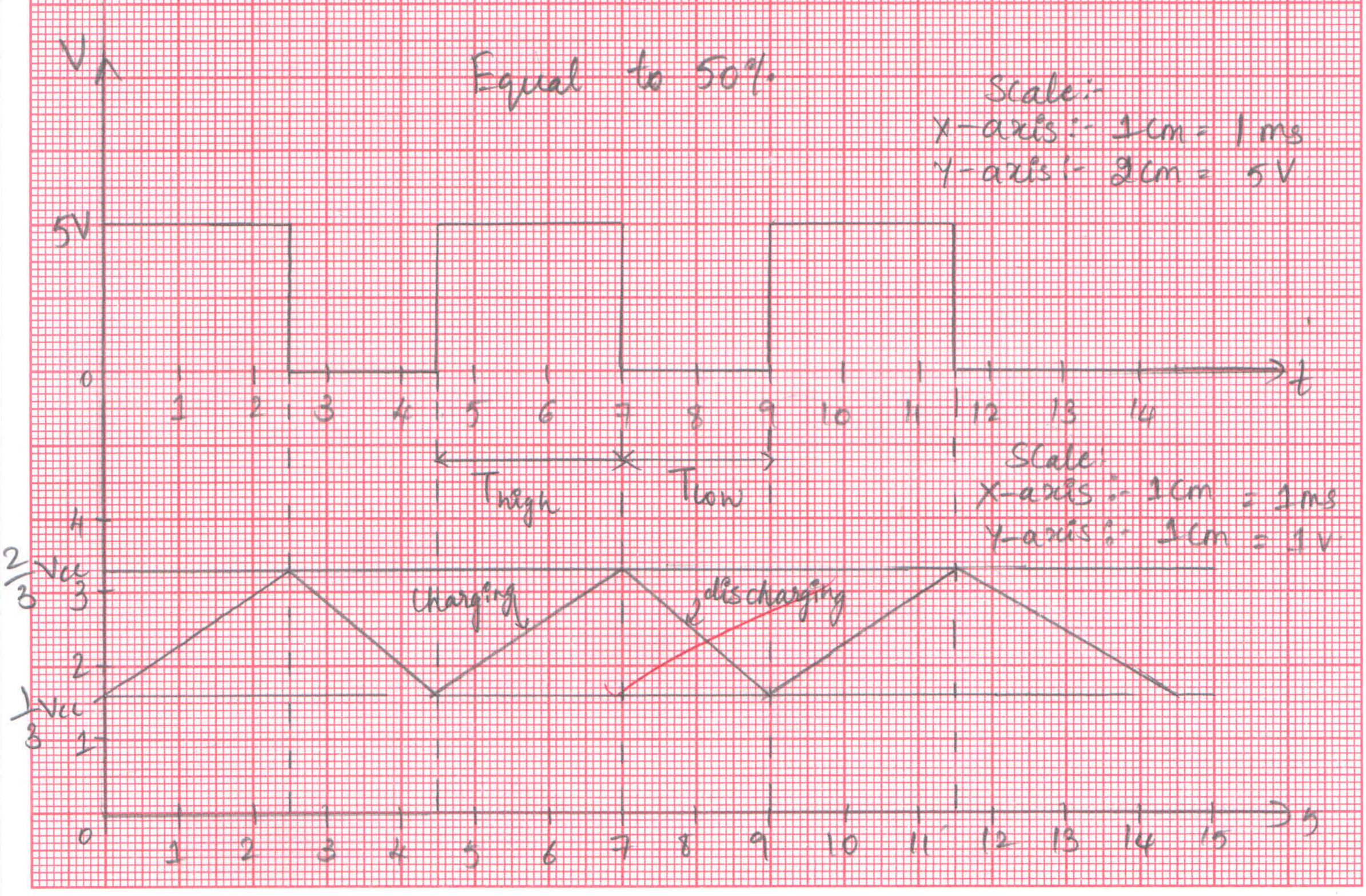
Tabular Column for Astablemultivibrator.

Duty cycle Theoretical	V_{p-p}	Thigh	Tlow	Duty cycle practical.	$V_{cc(p-p)}$
36%	5V	2 msec.	3.5 msec.	36.56%.	5 V.
50%	5V	2.5 msec.	2 msec.	55.56%	4.9 V
64%	5V.	4 msec.	2 msec.	66.67%.	4.6 V

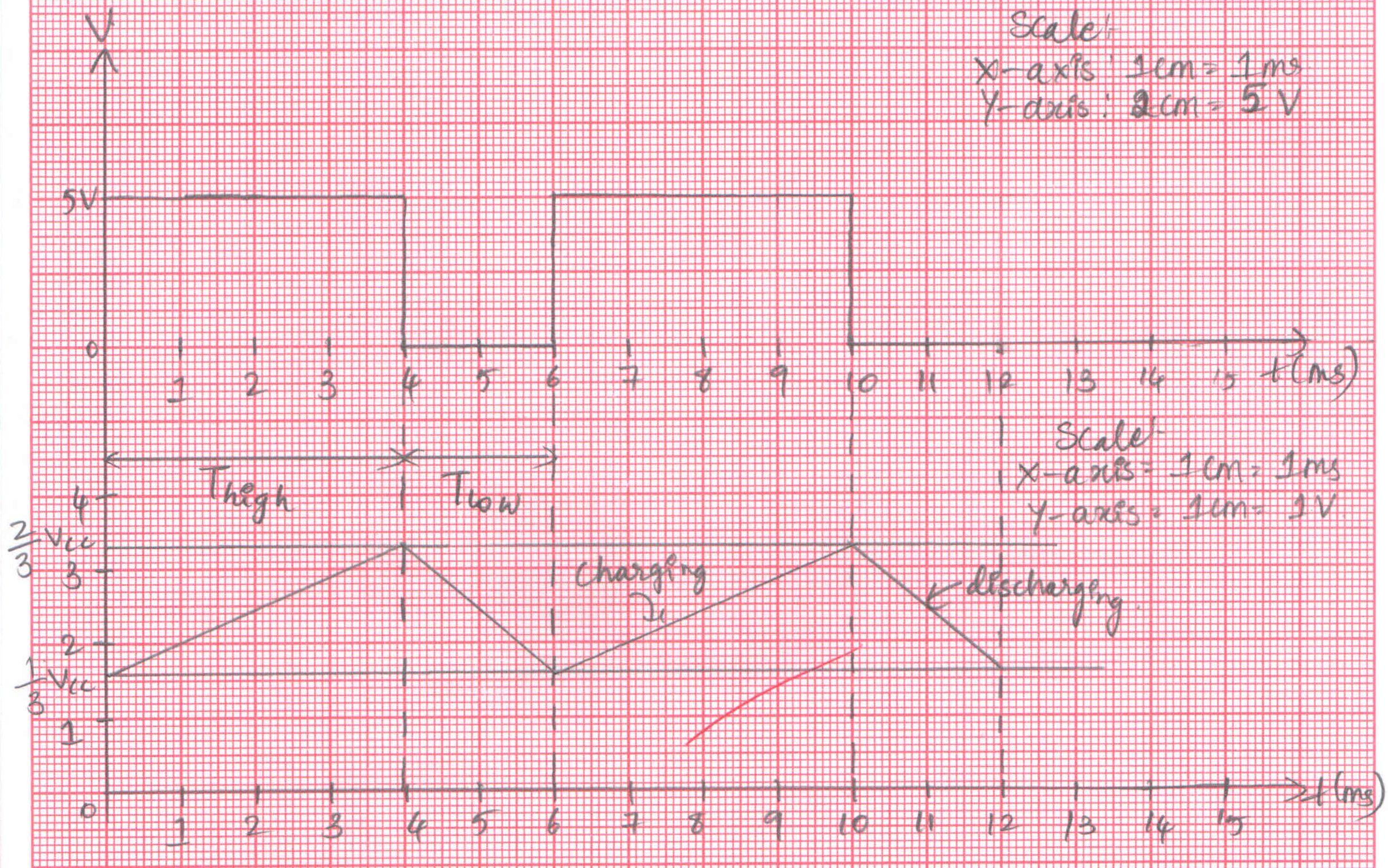
Less than 50% (36%)



Equal to 50%



More than 50% (64%)



(b) Monostable multivibrator.

Theory :-

A monostable multivibrator has one stable output state. Its normal output voltage may be high or low, and it stays in the normal state until triggered. When triggered, the o/p switches to the opposite state for a time dependent on the circuit components.

The dc conditions of the circuit are that the op-amp inverting input terminal is grounded via resistor R_3 and the non inverting input terminal is biased positively by resistor R_1 and R_2. Consequently the op-amp output is normally positive saturation level and the capacitor C_2 is charged with the polarity. If C_2 was not present, the circuit would be similar to capacitor-coupled voltage level detector that switches its o/p from $+V_o$ to $-V_{sat}$.

(b) Monostable multivibrator.

Design -

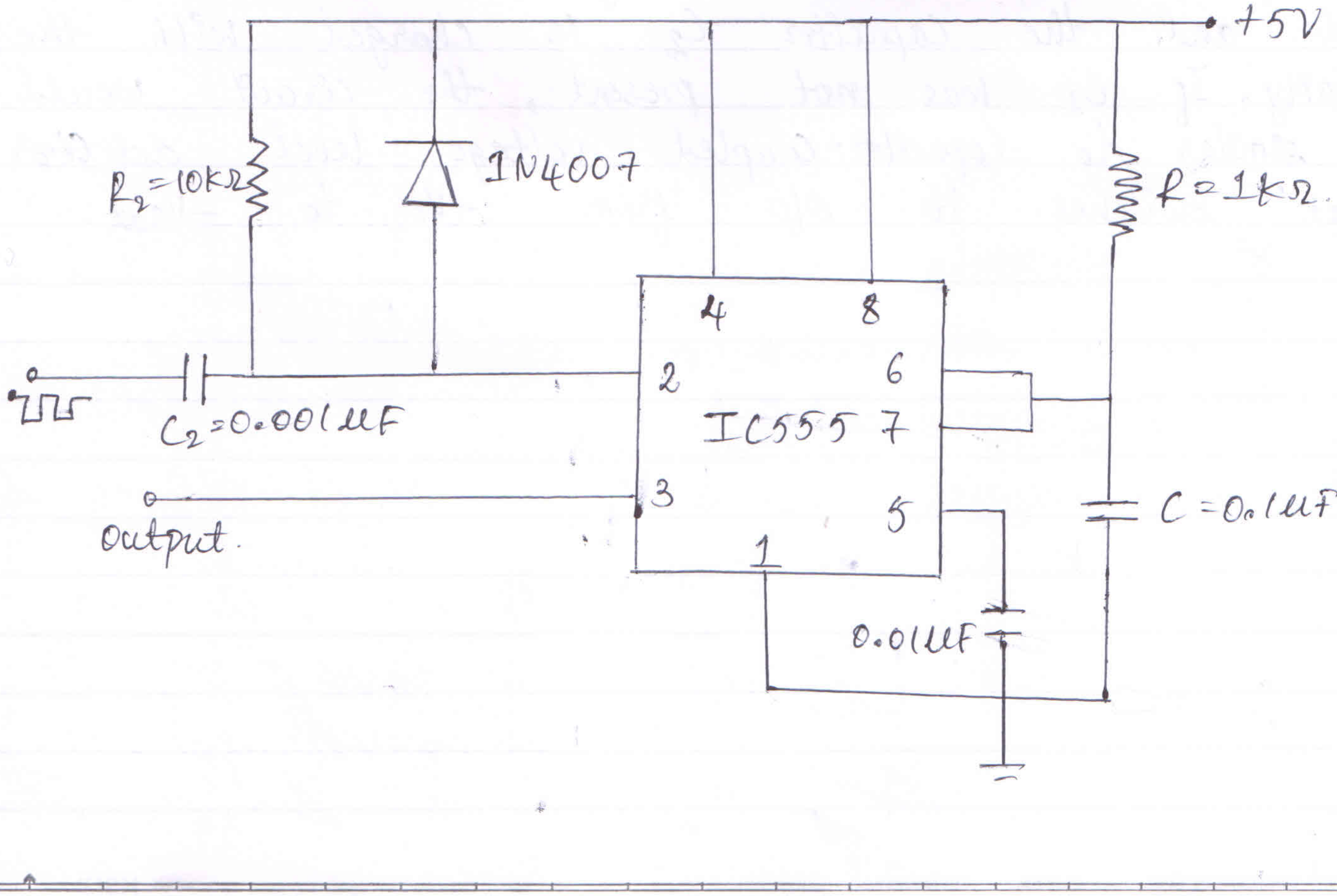
Trigger input of frequency 1kHz i.e, $T = 1$ msec.
let $t_p < T$. let $t_p = 0.1$ msec.

$$t_p = 1.1RC$$

let $C = 0.1\mu F$.

$$R = \frac{t_p}{1.1 \times C} = 1k\Omega.$$

Monostable Multivibrator.



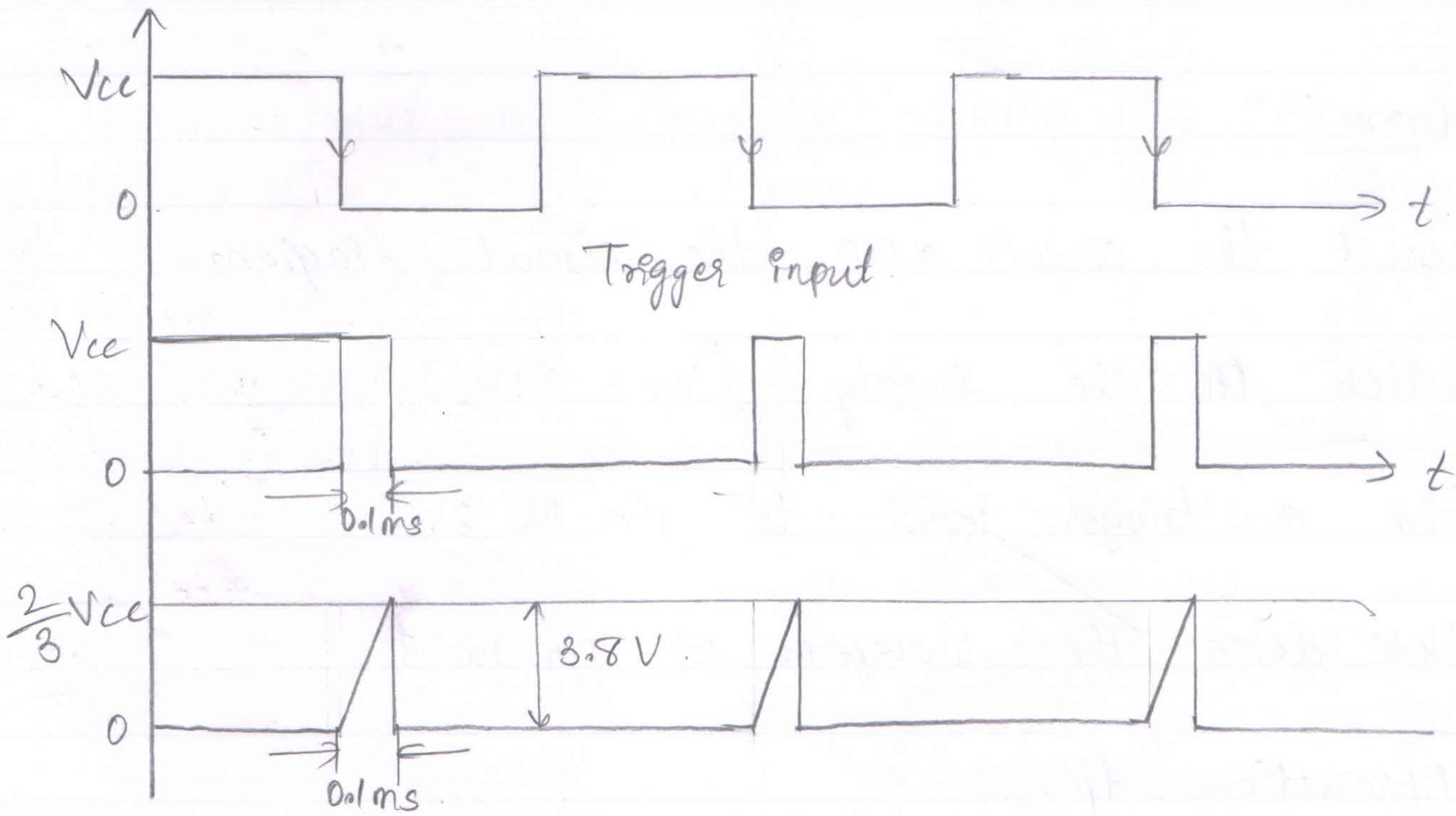
DATE 3/4/19
EXP. NO. 7

EXPT. TITLE : Astable and Monostable multivibrator

Procedure :-

1. Connect the circuit as per the circuit diagram.
2. Switch ~~On~~ the supply ($V_{cc} = 5V$).
3. Give a trigger Input to pin No 2.
4. Note down the waveform at pin no. 3.
5. Observation tp.

Waveforms:



DATE 3/4/19 EXPT. TITLE : PAGE NO. 2

Monostable multivibrator

Scale:-
X-axis:- 1cm = 0.5msec
Y-axis- 1cm = 5V



Scale:-
X-axis:- 1cm = 0.5ms
Y-axis - 1cm = 1V



Result :-

(a) Astable multivibrator for the given duty cycle has been verified.

(b) Monostable multivibrator for a given pulse width.

Theoretical pulse width, tp = 0.1msec.

Practical pulse width, tp = 0.1 msec.

	Marks obtained
Observation (10)	10
Record (10)	09
Viva (5)	03
Total (25)	22

Design :-

Modulation Design.

Given $f_c = 500$ KHz.

$$T = \frac{1}{f_c} = \frac{1}{500 \times 10^3} = 2 \mu sec$$

(a) To design Base Clamping Circuit.

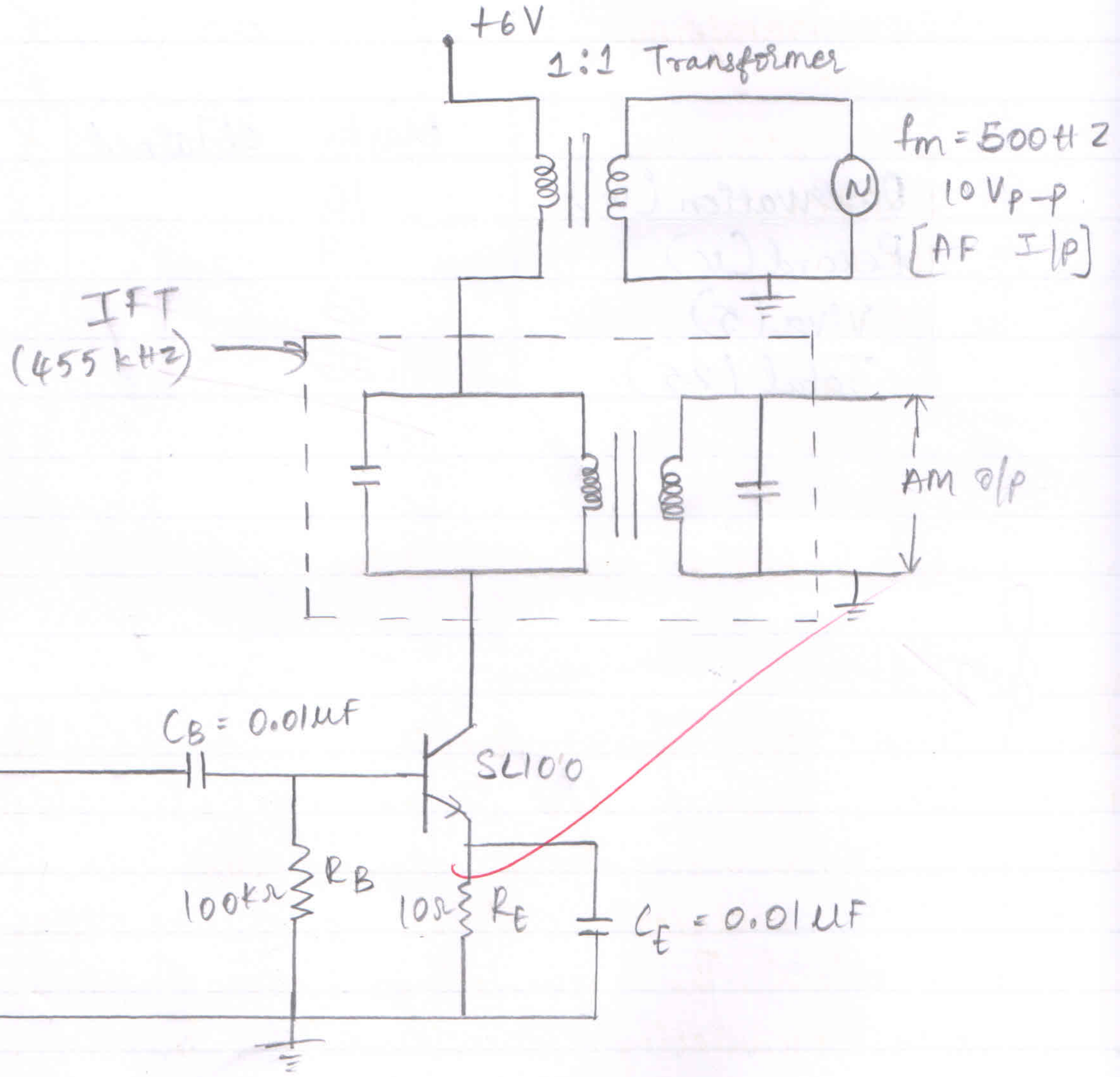
$$R_B C_B \gg 20T$$

That is $R_B C_B \gg 40 \mu sec$.

Let $R_B = 100$ K and $C_B = 0.01$ μf.

Therefore, $R_B C_B = 1000 \mu sec \gg 40 \mu sec$.

Collector Modulation (AM modulation)



DATE 24/4/19
EXP. NO. 8

EXPT. TITLE : Collector Amplitude Modulation

PAGE NO. 36

Aim :-

To design and construct an experiment for the generation and demodulation of A.M.

Components required :-

Sl. No	Components	Quantity
1.	Regulated Power supply 5V	1
2.	Function Generator	1
3.	CRO	1
4.	1:1 Transformer	1
5.	SL100	1
6.	IFT 455KHz	1
7.	Resistors :-	
	100 kΩ	1
	10 Ω	1
	39kΩ	1
	4.7 μF	1
	0.01 μF	3
8.	Bread board, Connecting Wires	1 set

Theory :-

Figure shows the basic circuit for a BJT modulator. It is a high power class C amplifier with high-level modulators. The modulator is a linear power amplifier that takes the low modulating signal and amplifier it to a high power level. The modulating output signal is coupled through modulating transformer T_1 to the class C

Demodulation Design.

$$\frac{1}{f_m} \gg R_c \gg \frac{1}{f_c}$$

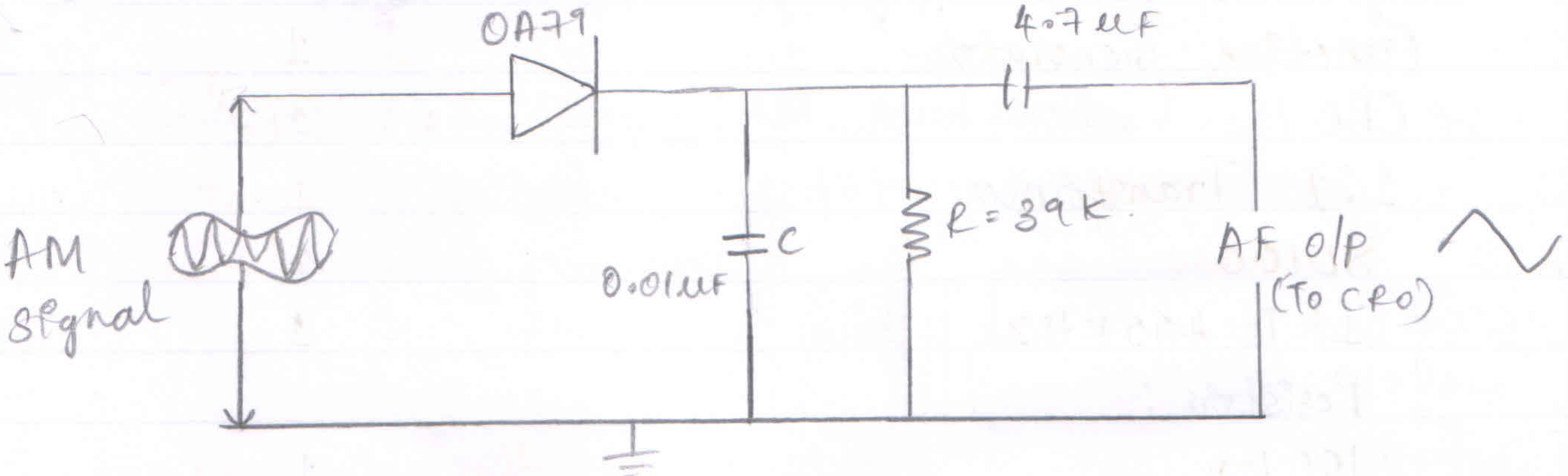
let $R_c \gg \frac{10}{f_c}$; $f_c = 455\ kHz$.

$f_m = 500\ hz$.

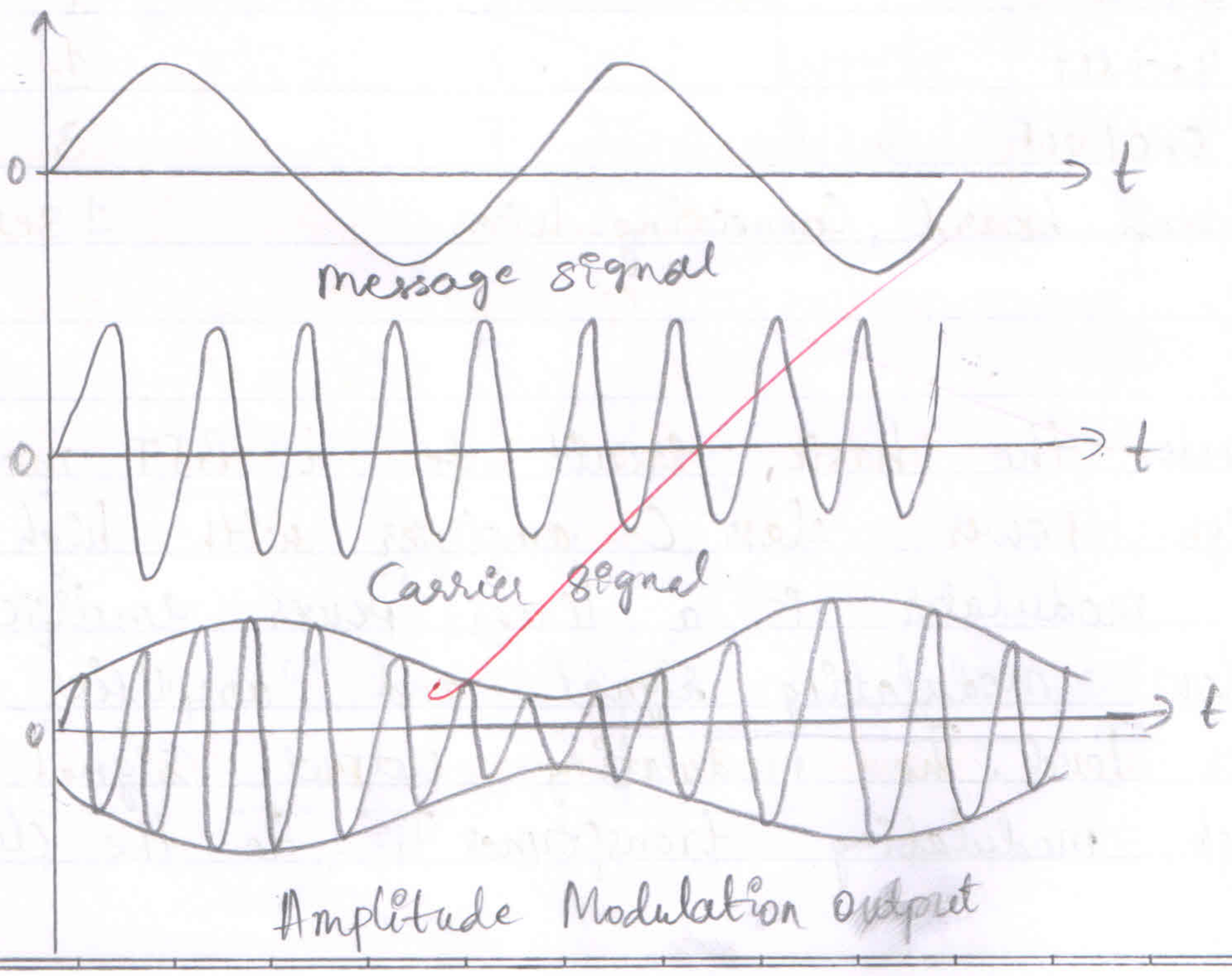
Choose $C = 0.01\ \mu F$

$R = 39k$. $R_c = 390\ \mu sec \gg 10/f_c$.

AM Demodulation.



Waveforms :-



amplifier. The secondary winding of the modulation transformer is connected in series with the collector supply voltage Vcc of the class C amplifier. This means that modulating signal is applied in series with the collector power supply voltage of the class C amplifier applying collector modulation.

In absence of modulating input signal, there will be zero modulation voltage across the secondary of T1. Therefore, the collector supply voltage will be applied directly to the class C amplifier generating current pulses of equal amplitude and the output of the tuned circuit will be a steady sine wave.

When the modulating signal occurs the a.c voltage across the secondary of the modulating transformer will be added and subtracted from the collector supply voltage. This varying supply voltage is then applied to the Class C amplifier, resulting in variation in the amplitude of the carrier sine wave in accordance with the modulated signal. Due to this amplitude of the current ptw pulses also vary in accordance with the modulating signal. The tuned circuit then converts the current pulses in to an amplitude-modulated wave as shown in figure.

Procedure :-

1. Connections are made as shown in the circuit diagram.

Observations:

Carrier Input Voltage = 10V (constant)

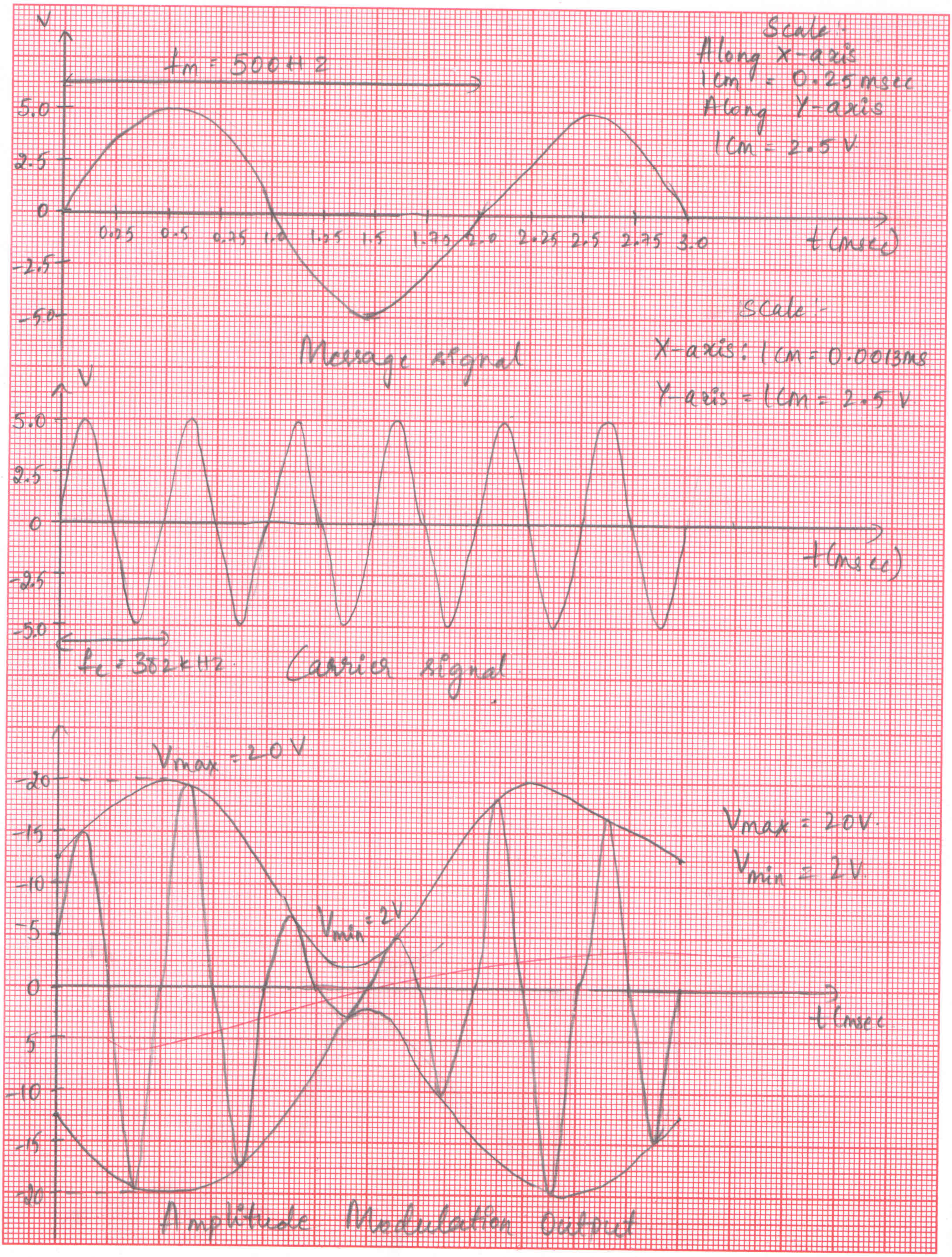
AF Ilp voltage = 10V (constant).

AF I/p. ~~V_i~~ = ~~f_i~~ =	Carrier I/p ~~V_c~~ = ~~f_c~~ =	Emax	Emin	$\%m = \frac{(E_{max} - E_{min})}{(E_{max} + E_{min})} \times 100$
V_i = 10V f_i = 500Hz	V_c = 10V f_c = 382kHz	20V	2V	$\%m = \frac{20-2}{20+2} \times 100$ $\%m = 81.81\%$

Output Voltage, V_o = 1.07 V at f = 500Hz.

Name :

Date : □□ □□ □□□□


V
f_m = 500 Hz
5.0
2.5
0
-2.5
-5.0
0.05 0.5 0.25 1.0 1.25 1.5 1.75 2.0 2.25 2.5 2.75 3.0
t (msec)
Scale :
Along X-axis
1cm = 0.25 msec
Along Y-axis
1cm = 2.5 V
Message signal
V
5.0
2.5
0
-2.5
-5.0
f_c = 352 kHz
t (msec)
Scale :-
X-axis : 1cm = 0.0013ms
Y-axis = 1cm = 2.5 V
Carrier signal
V_{max} = 20 V
V_{min} = 2V
20
15
10
5
0
5
10
15
20
t (msec)
V_{max} = 20V.
V_{min} = 2V.
Amplitude Modulation Output

DATE 24/9/19

EXP. NO. 8

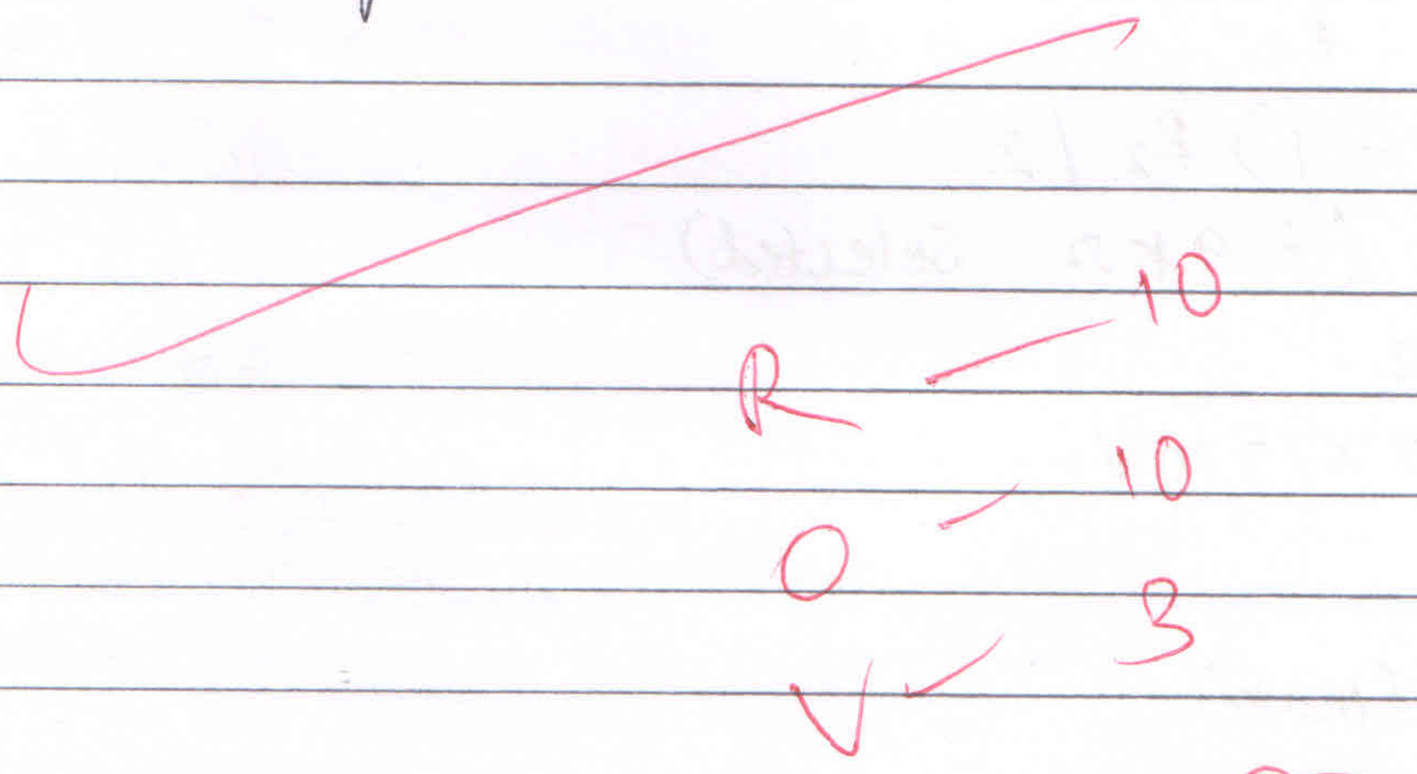
EXPT. TITLE : Collector Amplitude Modulation

2. Switch off the AFT (Modulating Input) of modulating signal. For Carrier frequency fc of the modulating signal, adjust the Carrier frequency to get max output.

3. Switch on the modulating signal and adjust amplifier about 5V pp, frequency to 1-2 kHz & obtain an undistorted amplitude modulated output.

Result :-

AM wave is generated and demodulated.



23

Sahana
24/9/19

Design :-

To design an instrumentation amplifier for an overall voltage gain of 900 with an input of 15 mV using 741 op-amps with a supply voltage of ±15 V.

Let $A_{V_1} \approx A_{V_2}$

$= \sqrt{A_V} = \sqrt{900}$

$= 30$

$I_2 \gg I_B(max)$

$I_2 \gg I_B(max) = 50\mu A$

$R_2 = \frac{V_i}{I_2} = \frac{15mV}{50\mu A} = 300\Omega$ (use 500Ω variable)

$A_V(diff) = \frac{2R_1 + R_2}{R_2}$

$R_1 = (A_V(diff) - 1) R_2 / 2.$

$= 4.35 k\Omega$ (3.9 kΩ selected)

$R_3 = R_1 = 3.9 k\Omega.$

$V_o = A_V V_i = 900 \times 15 mV.$

$= \mp 3.5 V.$

$I_5(min) \gg I_B(max)$

$I_5 = 100\, I_B(max) = 50\mu A$

$R_5 = \frac{V_o}{I_5} = \frac{13.59}{50\mu A} = 270 k\Omega$ (standard value)

$R_4 = \frac{R_5}{AV_2} = \frac{270 k\Omega}{30} = 9 k\Omega$ (select 8.2 kΩ standard value)

$R_6 = R_4 = 9 k\Omega$ (select 8.2 kΩ standard value)

$R_7 = R_5 \pm 20\% \approx 270 k\Omega \pm 20\%$

$= 216 k\Omega$ to $324 k\Omega$ (used 220 kΩ fixed ~~resistor~~)

DATE 8/5/19

EXP. NO. 9

EXPT. TITLE : Instrumentation Amplifier.

PAGE NO. 39

Aim :- To design an instrumentation amplifier of differential mode gain A using three amplifiers.

Components Requirement

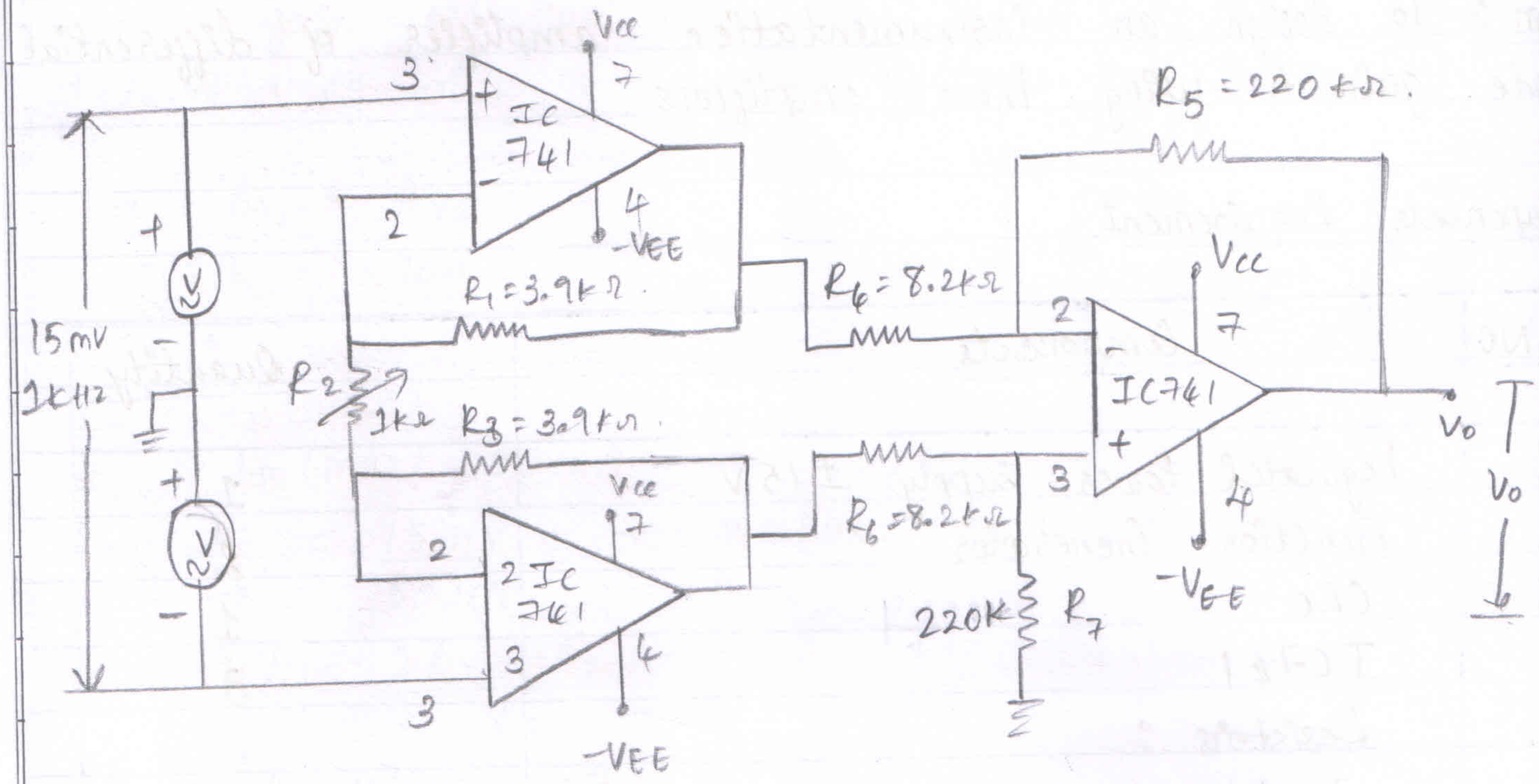
SI. NO	Components	Quantity
1	Regulated Power supply ±15V.	1
2.	Function Generator	2
3.	CRO	1
4.	IC741	3
5.	Resistors :	
	3.9kΩ	2
	8.2kΩ	2
	220kΩ	2
	1kΩ pot	1
6.	Bread board, Connecting Wires	1 set

Theory

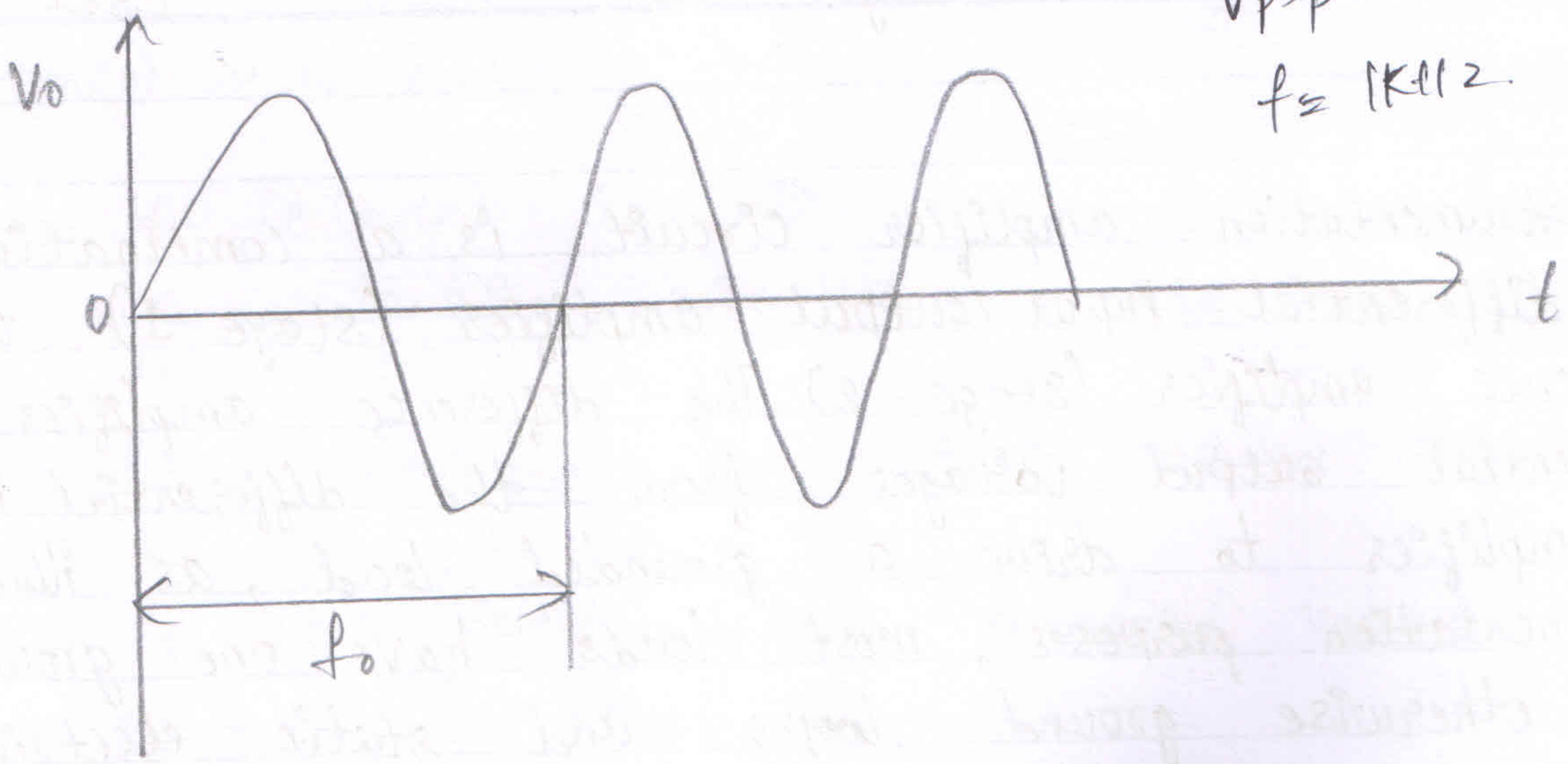
The instrumentation amplifier circuit is a combination of the differential input/output amplifier (stage 1) and the difference amplifier (stage 2). The difference amplifier uses the differential output voltages from the differential input/output amplifier to drive a grounded load, as illustrated. For instrumentation purposes, most loads have one grounded terminal, otherwise ground loops and static electricity could cause problems. So, the ability to drive a grounded load necessary. The differential input/output

Instrumentation Amplifier.

Circuit Diagram.



Expected Output.



$V_{p-p} = 26V$.

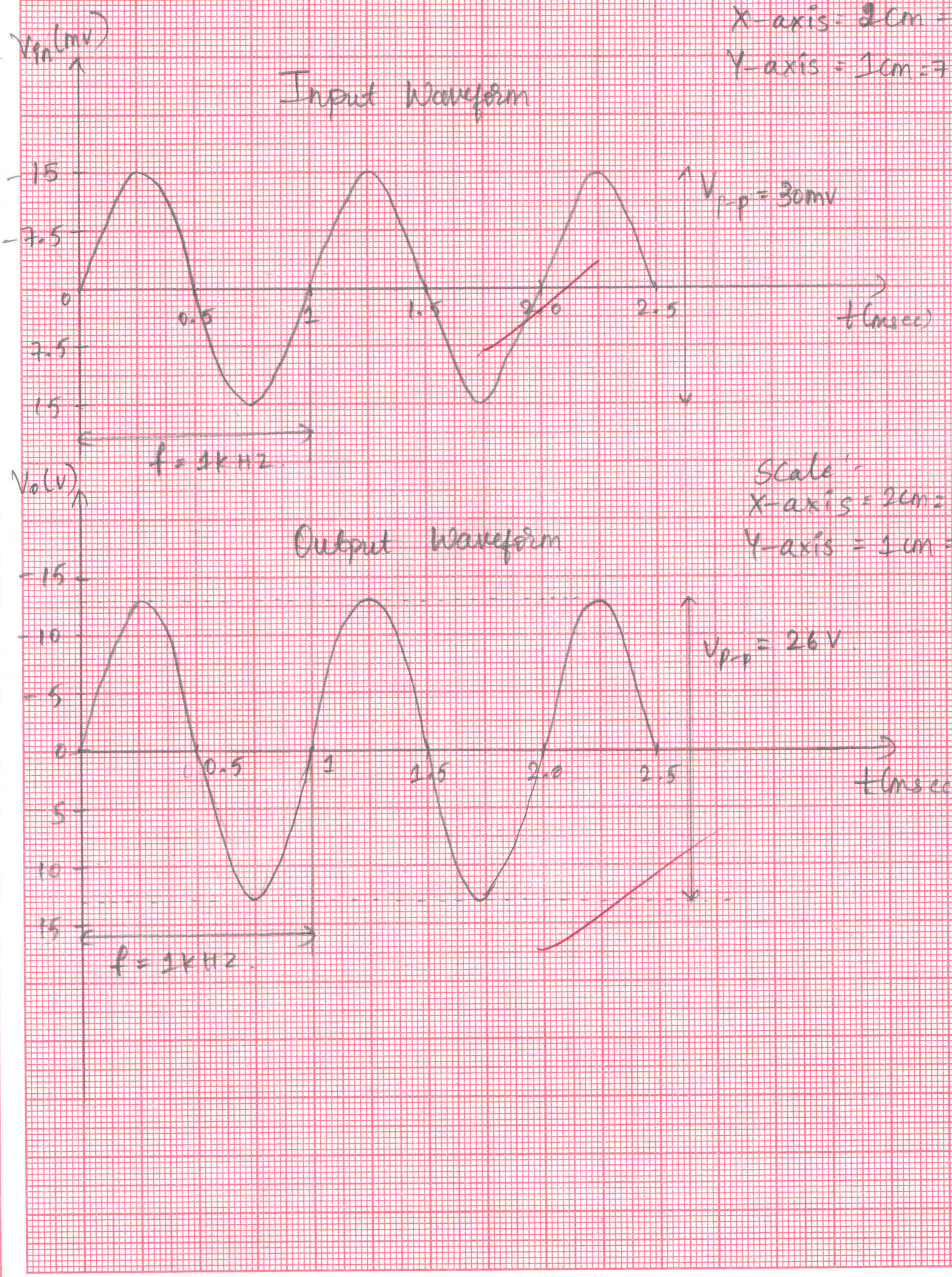
$f = 1KHz$.

Observations.

Input voltage V_i = 30 mv at 1kHz o/p vtg V_o = 26V at 1kH

Gain Av = 866.66

Scale:
X-axis: 2cm = 0.5msec
Y-axis = 1cm = 7.5mV



Scale:
X-axis = 2cm = 0.5msec
Y-axis = 1cm = 5V

stage offers a very high input resistance at each point input terminal.

Procedure :-

1. Connections are made as shown in the circuit diagram of fig 1.
2. Apply AC input sine wave of peak amplitude of 15 mV at a frequency of 1 KHZ from signal generators from the circuit shown.
3. Chelk the power supply of +15V and -15V.
4. Vary the pot and observe the output till you get $V_o \cong A_v V_i$. Measure the output voltage and Calculate A_v

Result :-

Theoretical and Practical Gain of the instrumentation amplifier are verified.

	Marks obtained
Observation (10)	08
Record (10)	08
Viva (5)	03
Total (25)	19

DATE 18/5/19

EXP. NO. 10

EXPT. TITLE : FM modulation & Demodulation

Aim :-

Demonstrate a suitable experiment to generate an FM signal using IC 8038 and its demodulation using IC565

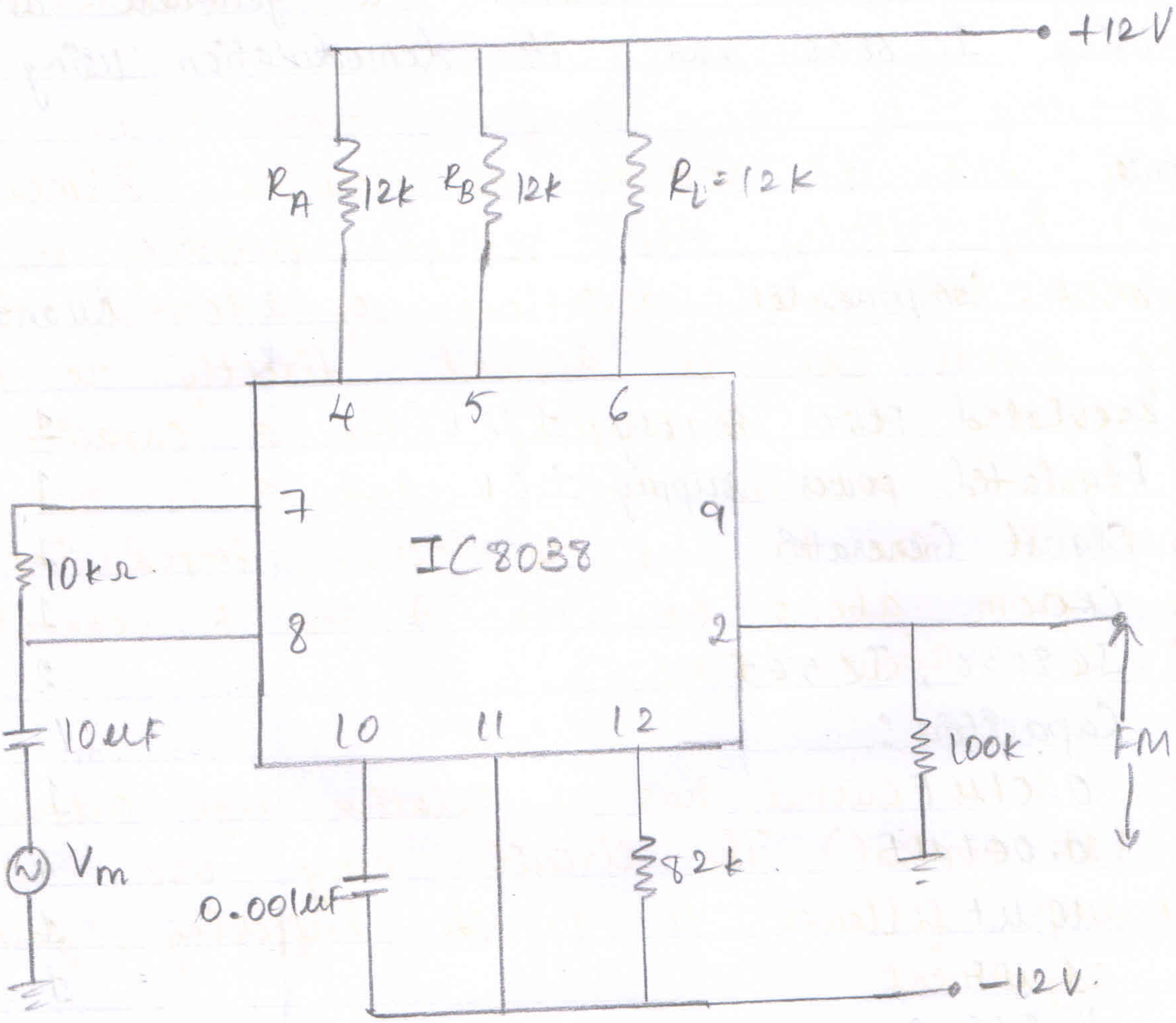
Requirements :-

SI NO	Components	Quantity
1.	Regulated power supply ±12 V.	1
2.	Regulated power supply ±6 V	1
3.	Signal Generator	1
4.	CRO	1
5.	Ic 8038, Ic 565	2
6.	Capacitors :	
	0.01μF	1
	0.001 μF	4
	10 μF	1
	1 μF	1
7.	Resistors :	
	12 kΩ	3
	82 kΩ	1
	100 kΩ	1
	10 kΩ	2
	1 kΩ	2
	47kΩ	1

Theory :-

The Ic 8038 waveforms generator is a monolithic

FM modulation Using IC 8038.



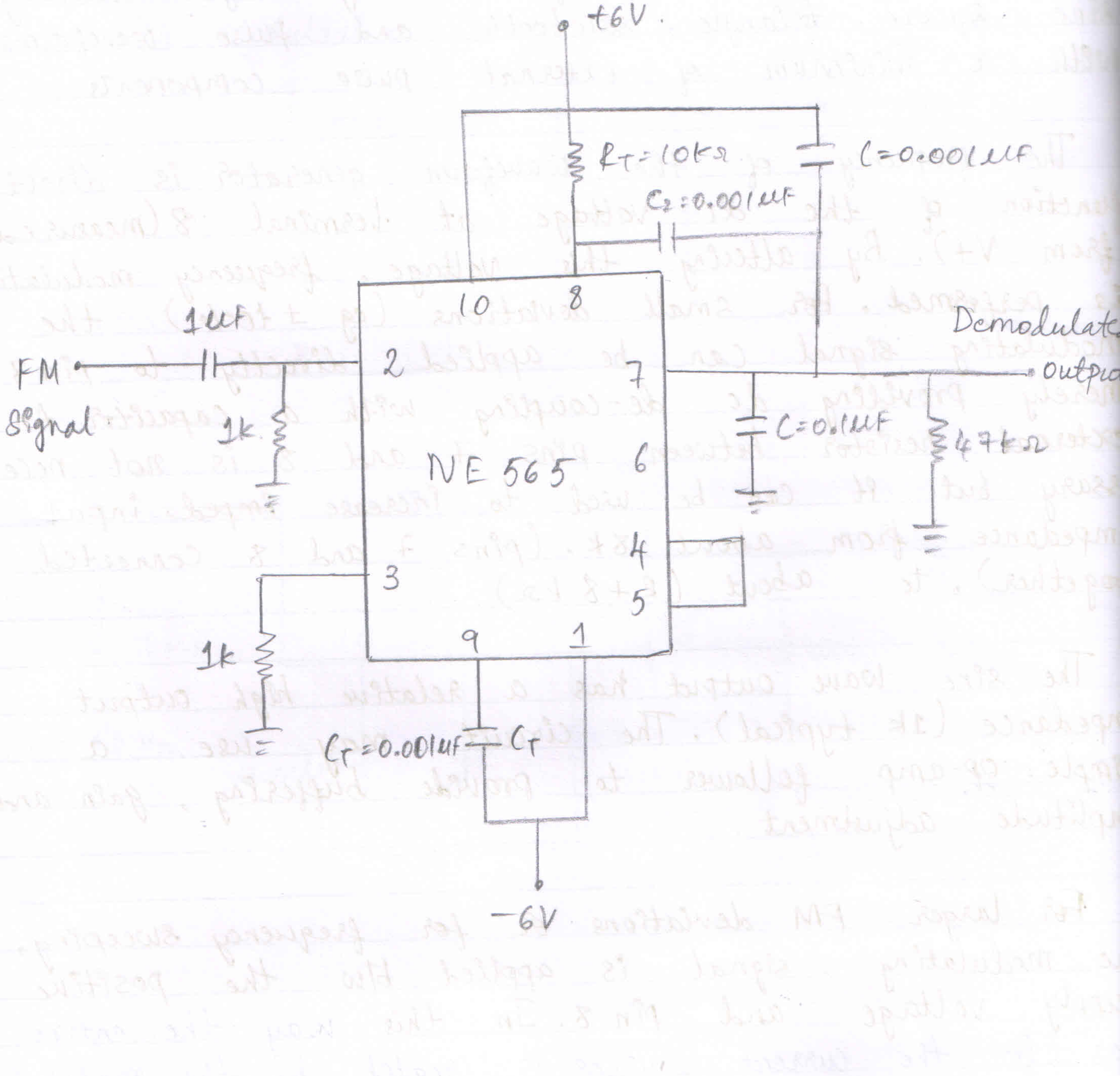
Integrated circuit capable of producing high accuracy sine, square, triangle, sawtooth and pulse waveforms with a minimum of external pulse components.

The frequency of the waveform generator is direct function of the dC voltage at terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (eg ± 10%) the modulating signal can be applied directly to pin 8, merely providing dc de-coupling with a capacitor. An external resistor between pins 7 and 8 is not nec-ssary but it can be used to increase ~~imped~~ input impedance from about 8k. (pins 7 and 8 connected together), to about (R + 8 kΩ).

The sine wave output has a relative high output impedance (1k typical). The circuit may use a simple op-amp follower to provide buffering, gain and amplitude adjustment.

For larger FM deviations or for frequency sweeping, the modulating signal is applied b/w the positive supply voltage and pin 8. In this way the entire bias for the current sources is created by the modulating, and a very large (eg. 1000:1) sweep range is created (f = 0 at $V_{sweep} = 0$). Care must be taken, however, to regulate the supply voltage, in this configuration the charge current and thus the frequency becomes dependent on the supply voltage. The potential on pin 8 may

Frequency Demodulation Circuit Diagram.



be swept down from V+ by (7/3 V_{supply} - 2V).

The IC 8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations.

Features -

- Low-frequency drift with temperature
- Simultaneous sine, square and triangular wave o/p's.
- Low distortion sine wave output.
- High linearity triangle wave output.
- Wide operating frequency range 0.001 HZ to 300KHz
- High-level output - TTL to 28V.
- Easy to use-just a handful of external components required.

Procedure :-

1. Connections are made as shown in the circuit diagram.

2. Apply +12V & -12V to the Ic 8038 as supply voltage from regulated power supply.

3. For the modulation circuit observe the carrier waveform at pin number 2 by switching off the function generator. Note the carrier frequency.

4. Switch on function generator and apply a modulating

Calculations -

Frequency deviation $\Delta f = f_2 - f_1$

$f_2 = 50$ kHz.

$f_1 = 16.67$ kHz.

$\Delta f = f_2 - f_1 = 33.33$ kHz.

Modulation index $\beta = \frac{\Delta f}{f_m}$

$$\beta = \frac{33.33 \text{ kHz}}{1 \text{ kHz}} = 33.33$$

Transmission bandwidth $B_T = 2(\Delta f + f_m)$.

$B_T = 2(33.33 \text{ kHz} + 1 \text{ kHz})$

$= 68.67$ kHz

DATE 8/5/19 | EXPT. TITLE : FM Modulation & Demodulation | PAGE NO. 44

EXP. NO. 10

signal of 2V peak to peak and frequency in the range of 1khz to 10khz through RC circuit as shown.

5. Observe FM output at pin 2 and measure f_1 & f_2.

6. Calculate frequency deviation Δf, modulation index β and transmission bandwidth B_T.

7. For FM demodulation, connections are made as shown in circuit diagram.

8. Apply +6V and -6V to the IC565 as supply voltage from regulated power supply.

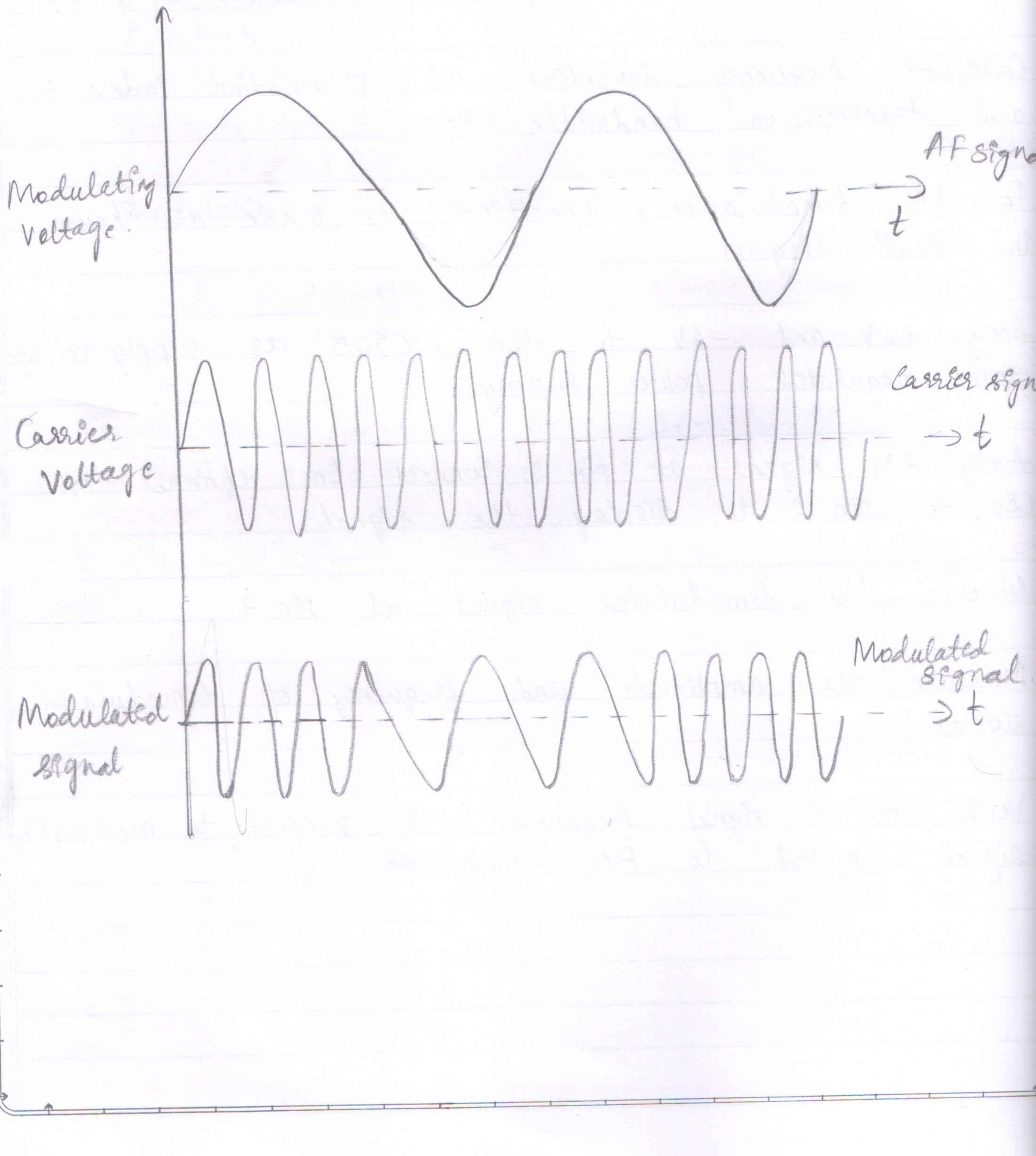
9. Apply FM signal at pin 2. Connect one channel of CRO to pin 2 to display the signal.

10. Observe the demodulated signal at pin 7.

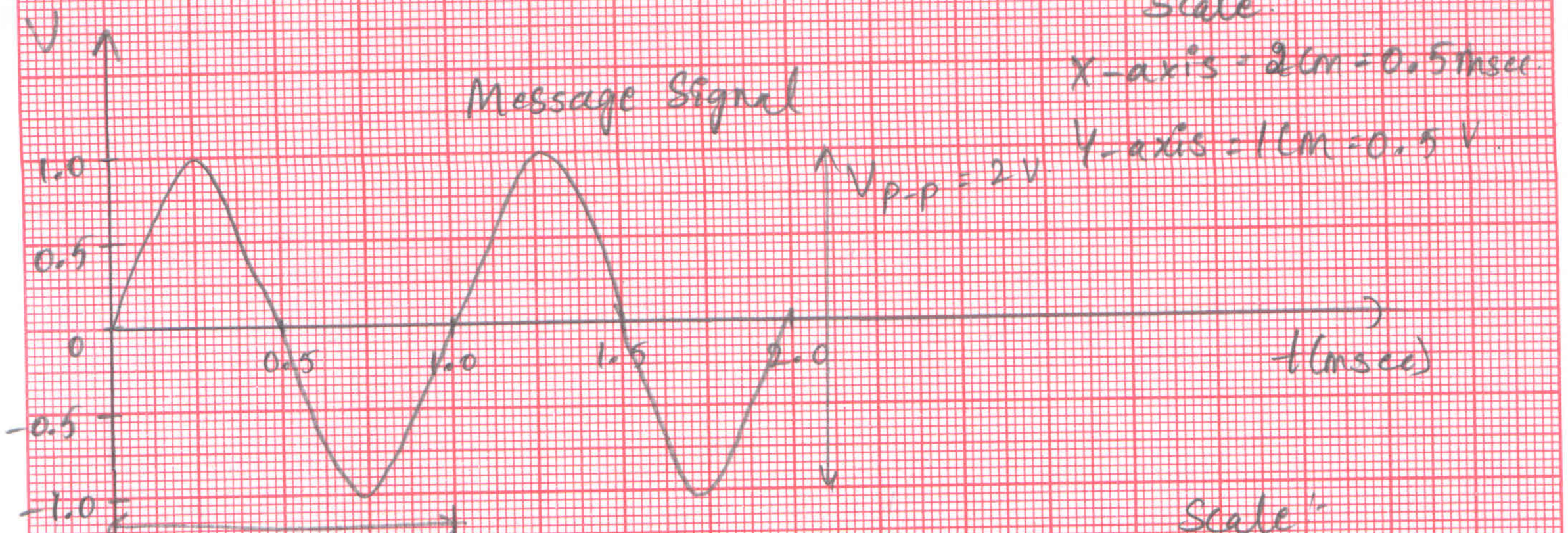
11. Measure the amplitude and frequency of demodulated signal.

12. Verify output signal frequency with respect to modulating signal applied to FM modulator.

Waveforms :-

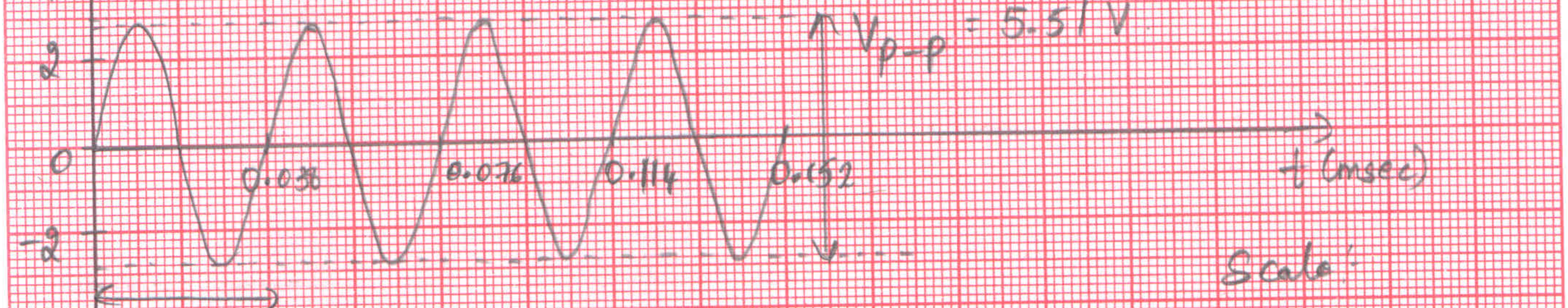

Modulating Voltage
AF signal
t
Carrier Voltage
Carrier signal
t
Modulated signal
Modulated signal
t

Message Signal



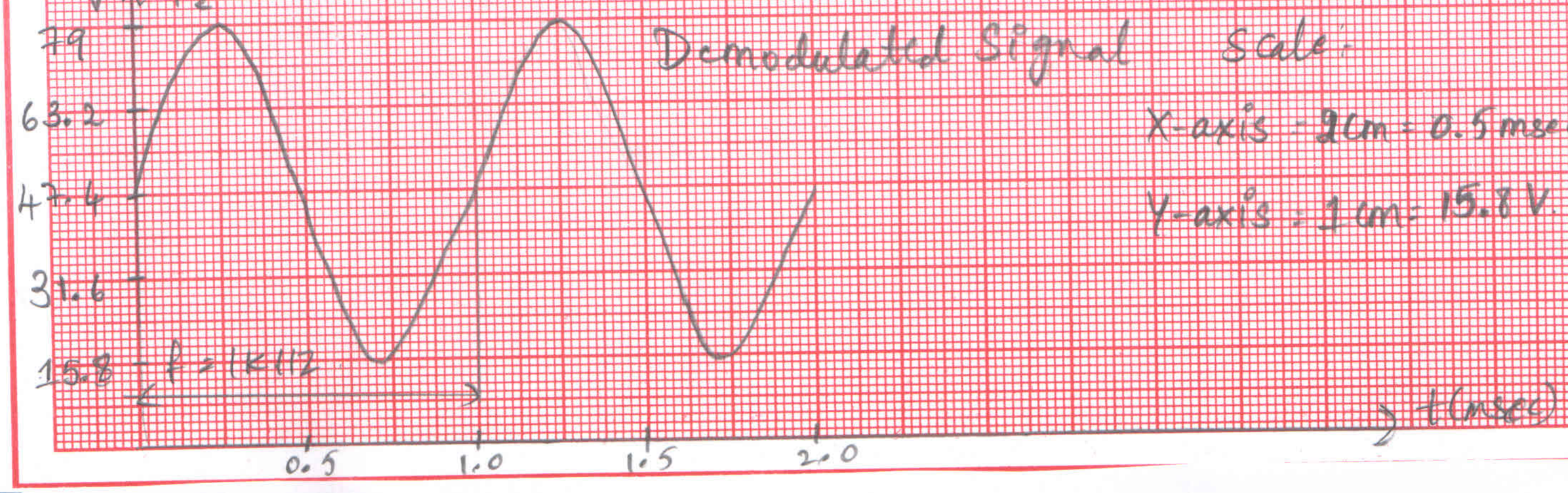
Scale:
X-axis = 2cm = 0.5msec
Y-axis = 1cm = 0.5 V

Modulated Signal



Scale:
X-axis = 2cm = 20 μsec
Y-axis = 1cm = 1.4 V

Demodulated Signal



Scale:
X-axis = 2cm = 0.5 msec
Y-axis = 1cm = 15.8 V.

Result :-

FM wave is generated using IC 8038 with Modulation index $\beta = 33.33$.

Transmission BW $B_T = 68.67$ KHz.

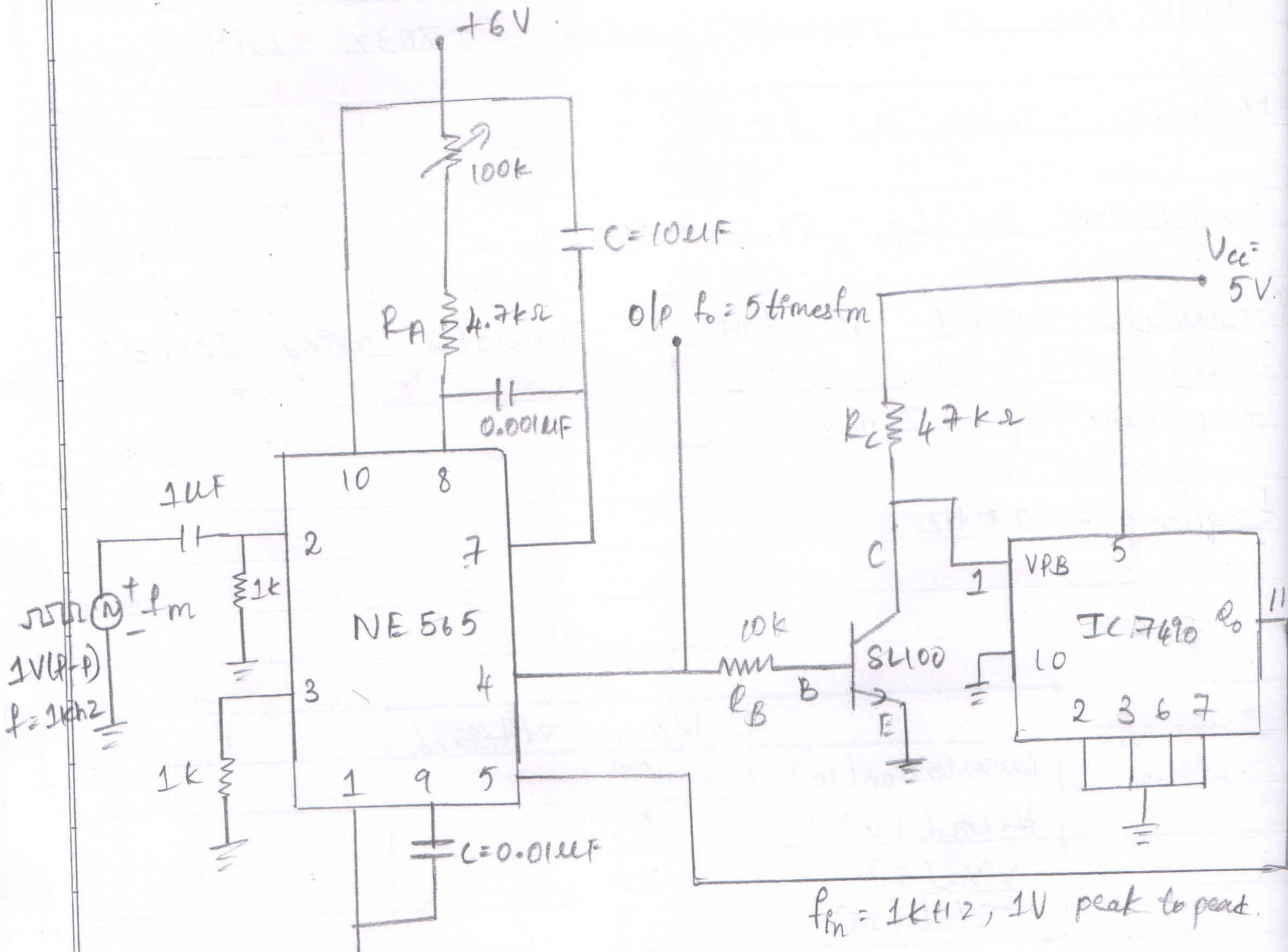
Demodulated signal for FM is generated using IC565 with

Amplitude = 63.2 mV.

Frequency = 1 KHz.

	Marks obtained.
Observation (10)	08
Record (10)	08
Viva (5)	03
Total (25)	19

Frequency Synthesizer Using PLL



DATE 10/5/19
EXP. NO. 11

EXPT. TITLE : Frequency Synthesis Using PLL

Aim :-

Conduct a suitable experiment to implement a frequency synthesizer circuit using IC 565 (PLL).

Components Required :

S.No	Components	Quantity
1.	Regulated Power supply 5V.	1
2.	Regulated Power supply ±6V	1
3.	Signal Generator	1
4.	CRO	1
5.	ICNE565	1
6.	Transistor SL100	1
7.	Capacitor : 0.01 μF, 0.001 μF, 10μF, 1μF	Each 1
8.	Resistors :	
	100 kΩ Pot	1
	10kΩ	1
	1kΩ	2
	4.7kΩ	2
9.	Bread board, Connecting Wires	

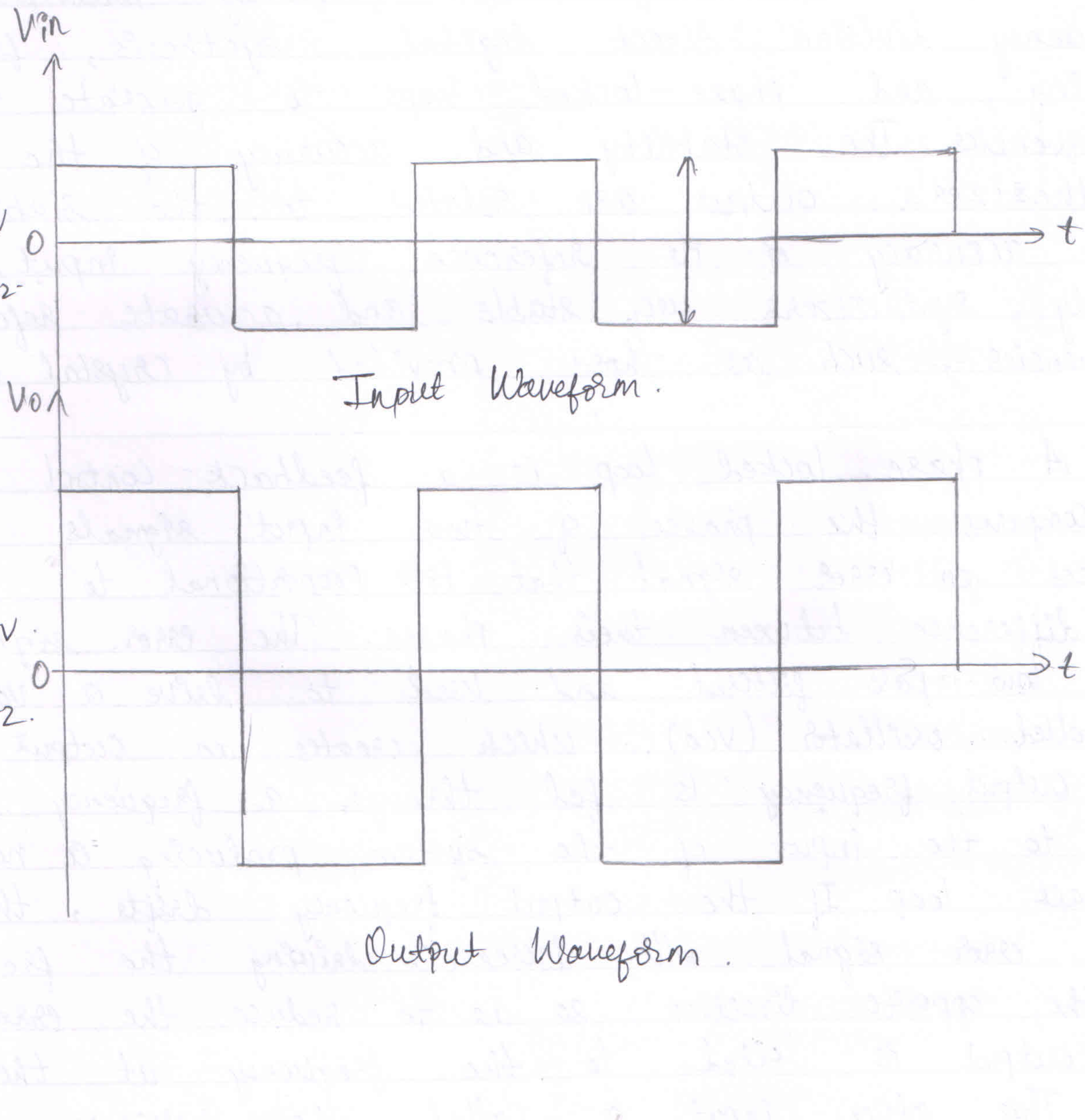
Theory :-

A frequency synthesizer is an electronic circuit that generates a range of frequencies from a single reference frequency. Frequency synthesis are used in many modern devices such as radio receivers, televisions, mobile telephones, radiotelephones, walkie-talkies,

CB radios, cable television converter boxes satellite receivers, and GPS systems. A frequency synthesizer may use the techniques of frequency multiplication, frequency division, direct digital synthesis, frequency mixing, and phase-locked loops to generate its frequencies. The stability and accuracy of the frequency synthesizer's output are related to the stability and accuracy of its reference frequency input. Consequently, synthesizers use stable and accurate reference frequencies, such as those provided by crystal oscillators.

A phase locked loop is a feedback control system. It compares the phases of two input signals and produces an error signal that is proportional to the ~~dff~~ difference between their phases. The error signal is then low pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the phase error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the output is locked to the frequency at the other input. This other input is called the reference and is usually derived from a crystal oscillator, which is very stable in frequency. The block diagram below shows the basic elements and arrangement of a PLL based frequency synthesizer.

Frequency Synthesis Waveforms :-

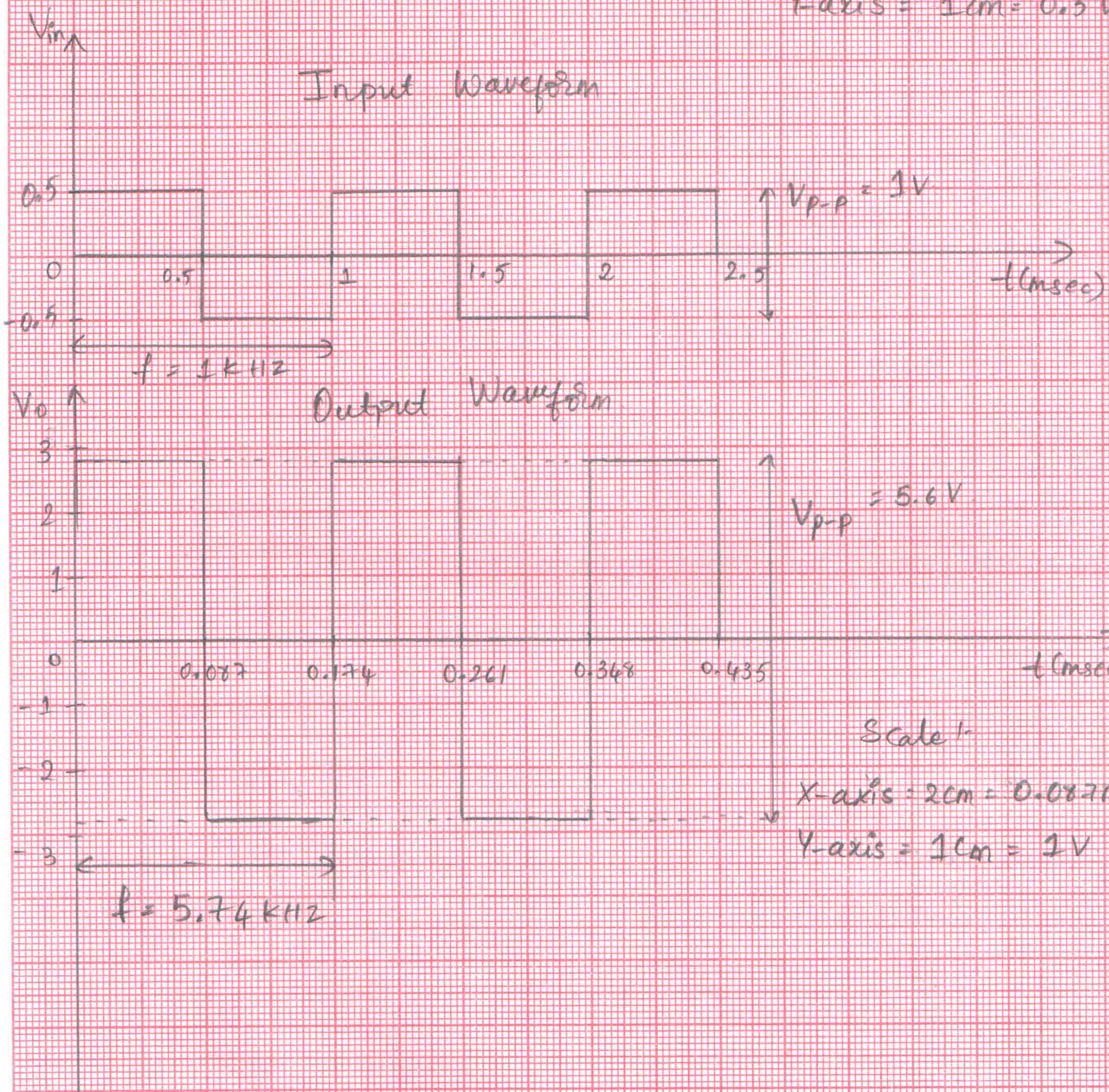


Input Waveform.

Output Waveform.

DATE 10/5/19 EXPT. TITLE :

Scale :
X-axis = 2cm = 0.5 msec
Y-axis = 1cm = 0.5 V



Scale :
X-axis : 2cm = 0.087ms
Y-axis = 1cm = 1V

DATE 10/5/19

EXP. NO. 11

EXPT. TITLE : Frequency Synthesis Using PLL

Procedure :-

1. Make connections as shown in circuit diagram.

2. Insert MOD-5 counter between pin 4 and 5 using SL100 to IC 565 as shown.

3. Using function generators at pin 2 apply square wave signal of 1 kHz frequency to get 1V p-p input signal.

4. By adjusting potentiometer 100K set the VCO frequency till PLL is locked, measure and note down the output frequency at pin no 4. It should be 5 times the input frequency.

5. Measure the amplitude and frequency of the output signal.

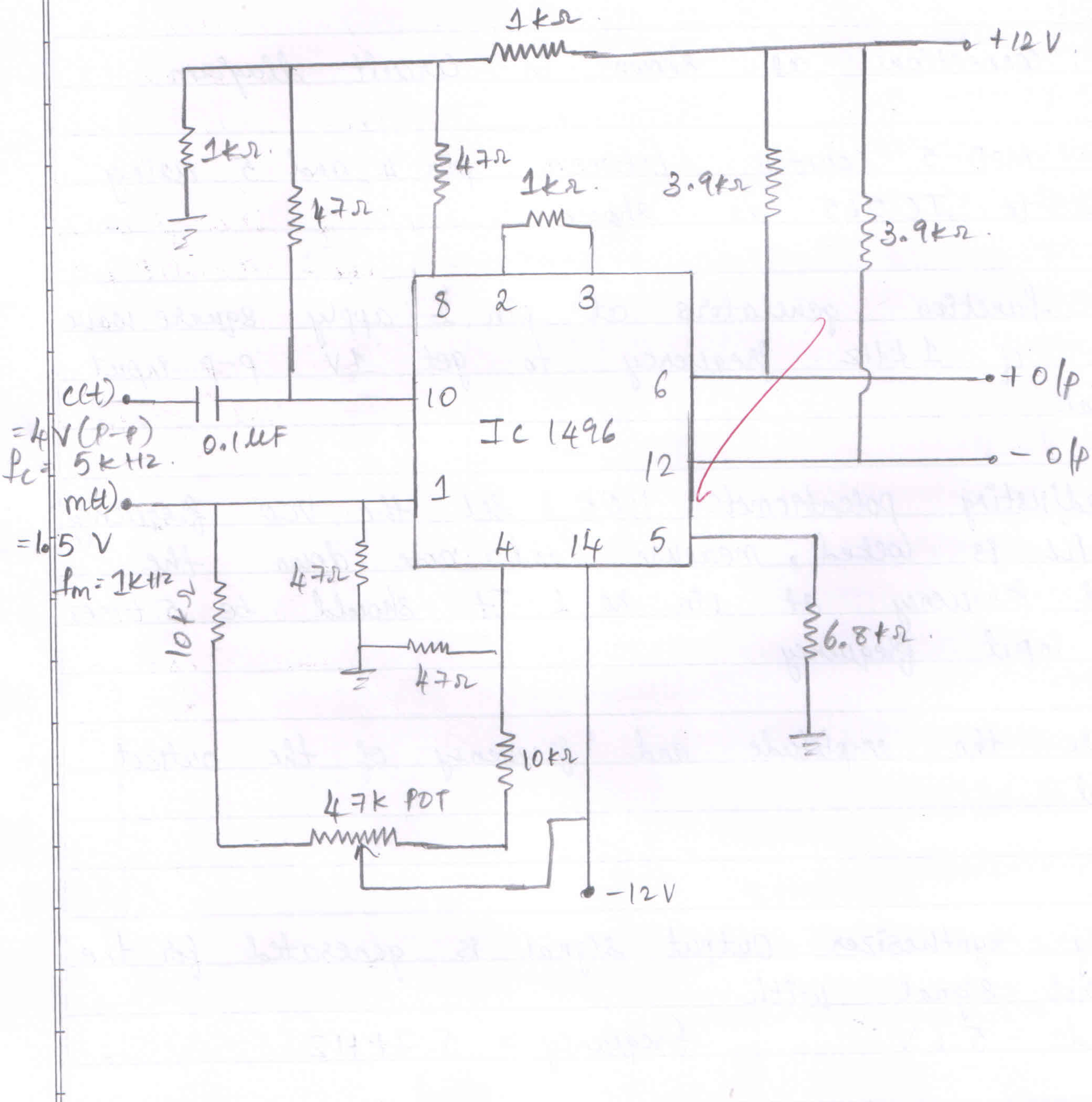
Result :-

Frequency synthesizer output signal is generated for the given input signal with

Amplitude = 5.6 V. Frequency = 5.7kHz.

	Marks Obtained
Observation (10)	08
Record (10)	08
Viva (5)	03
Total (25)	19

Balanced Modulator Using IC 1496.



DATE 10/5/19

EXP. NO. 12

EXPT. TITLE : Balanced Modulator Using IC 1496

PAGE NO. 49

Aim :-

Using IC 1496 reg up a balanced modulator circuit test its operation and record the waveform.

Components Requirement :-

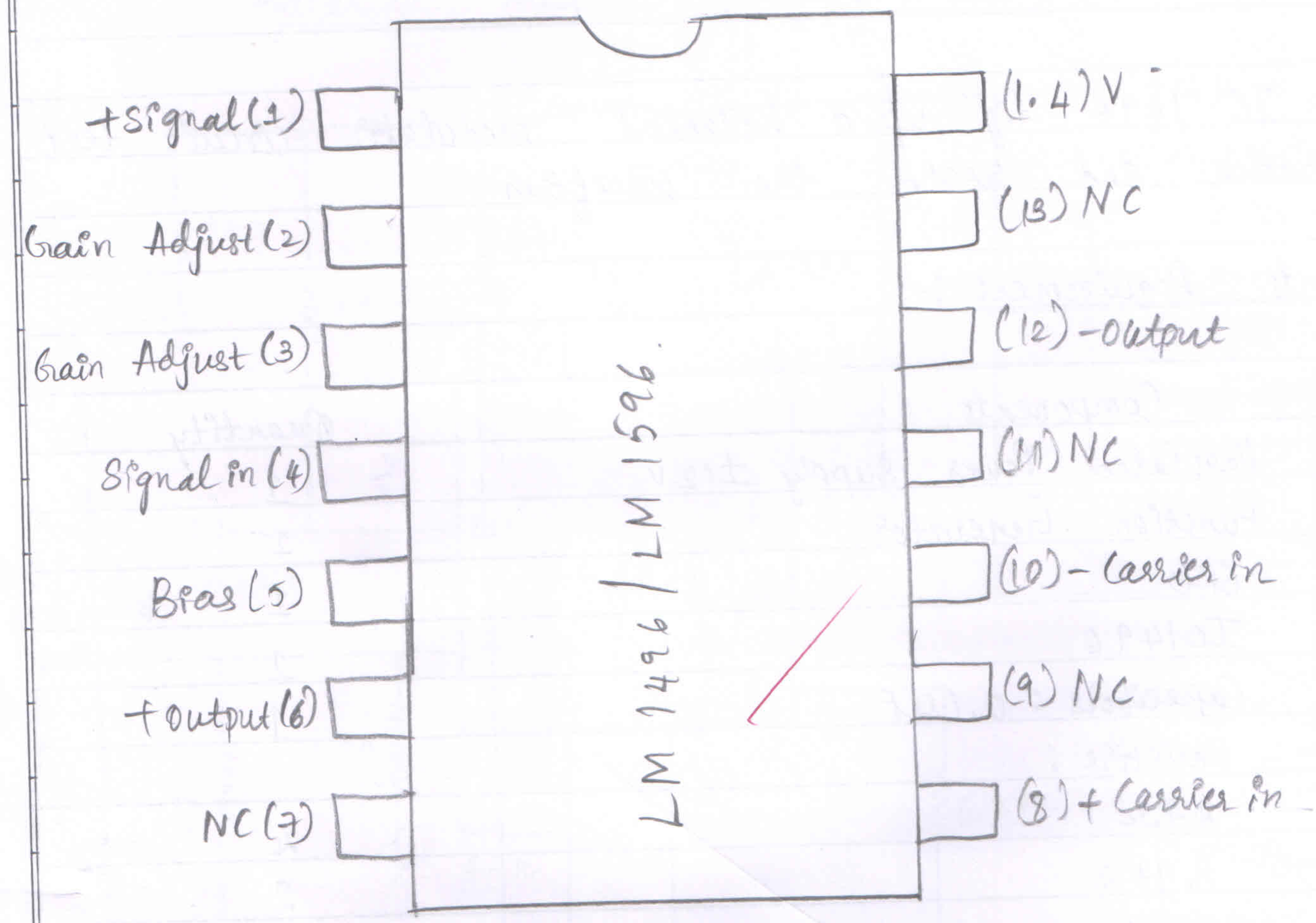
SI.NO	Components	Quantity
1.	Regulated Power supply ±12V.	1
2.	Function Generator	1
3.	CRO	1
4.	IC1496	1
5.	Capacitors : 0.1μF	1
6.	Resistors :	
	47Ω	4
	3.9kΩ	2
	6.8kΩ	1
	10kΩ	2
	1kΩ	3
	47kΩ Pot	1
7.	Bread board, Connecting Wires	1 set

Theory :-

The integrated circuit (IC) balanced mixer is widely used in receiver ICs, as well as being available as a separate integrated circuit. The IC versions are usually described as balanced modulation since the modulation function is basically the same as the mixing function.

Integrated circuit doubly balanced modulation like

Pin Details.



LM 1496 Top View.

the LM1496 operates as multiplier circuits that produce only side band pairs at the output. Application is simple, required only bias and an approximate band filter to eliminate side band pairs at harmonics of the carrier very little adjustment is required to obtain good balance.

An important advantage of the integrated circuit balanced modulator is that, when it is operated with a large carrier signal, the output signal amplitude is independent of the carrier amplitude. The result is the output amplitude depends only on the amplitude of the input signal (which is the modulating signal when it is used as a modulator or the side band signal when it is used as a demodulator)

General Description.

LM1596/LM1496 balanced Modulator-Demodulator:

The LM1596/LM1496 are double balanced modulator-demodulators which produce an output voltage proportional to the product of an input (signal) voltage and a switching (carrier) signal. Typical applications include suppressed carrier modulation, amplitude, synchronous detection, FM or PM detection board band frequency doubling and chopping LM1496 is specified for operation over the 0°c to +70°c temperature range.

DATE 10/5/19

EXP. NO. 12

EXPT. TITLE : Balanced Modulator Using IC LM1496

Features

- Excellent carrier suppression.
  65dB typical at 0.5MHZ.
  60dB typical at 10 MHZ.
- Adjustable gain and signal handling.
- Fully balanced input and output.
- low offset and drift.
- Wide frequency response up to 100 MHZ.

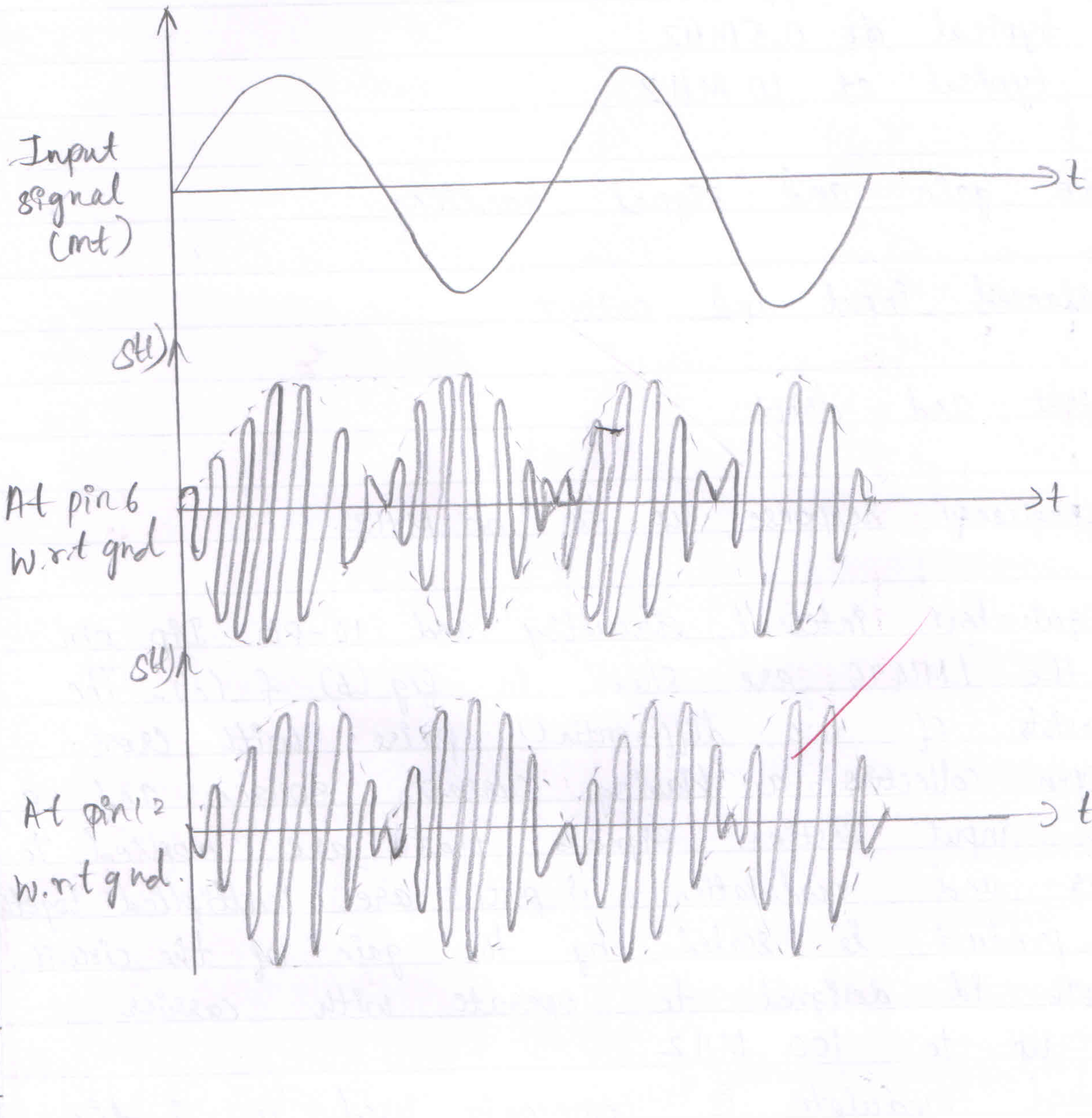
The equivalent internal circuitry and 14-pin Dip pin out for the LM1496 are shown in fig (b) & (c). The circuit consists of two differential pairs with cross-coupled open collectors a biasing current source, and a modulation input section signals that are applied to the carrier and modulation inputs are multiplied together, and the product is scaled by the gain of the circuit. The LM1496 id designed to operate with carrier frequencies up to 100 MHZ.

Balanced modulator is commonly used in radio transmitter and receiver circuitry.

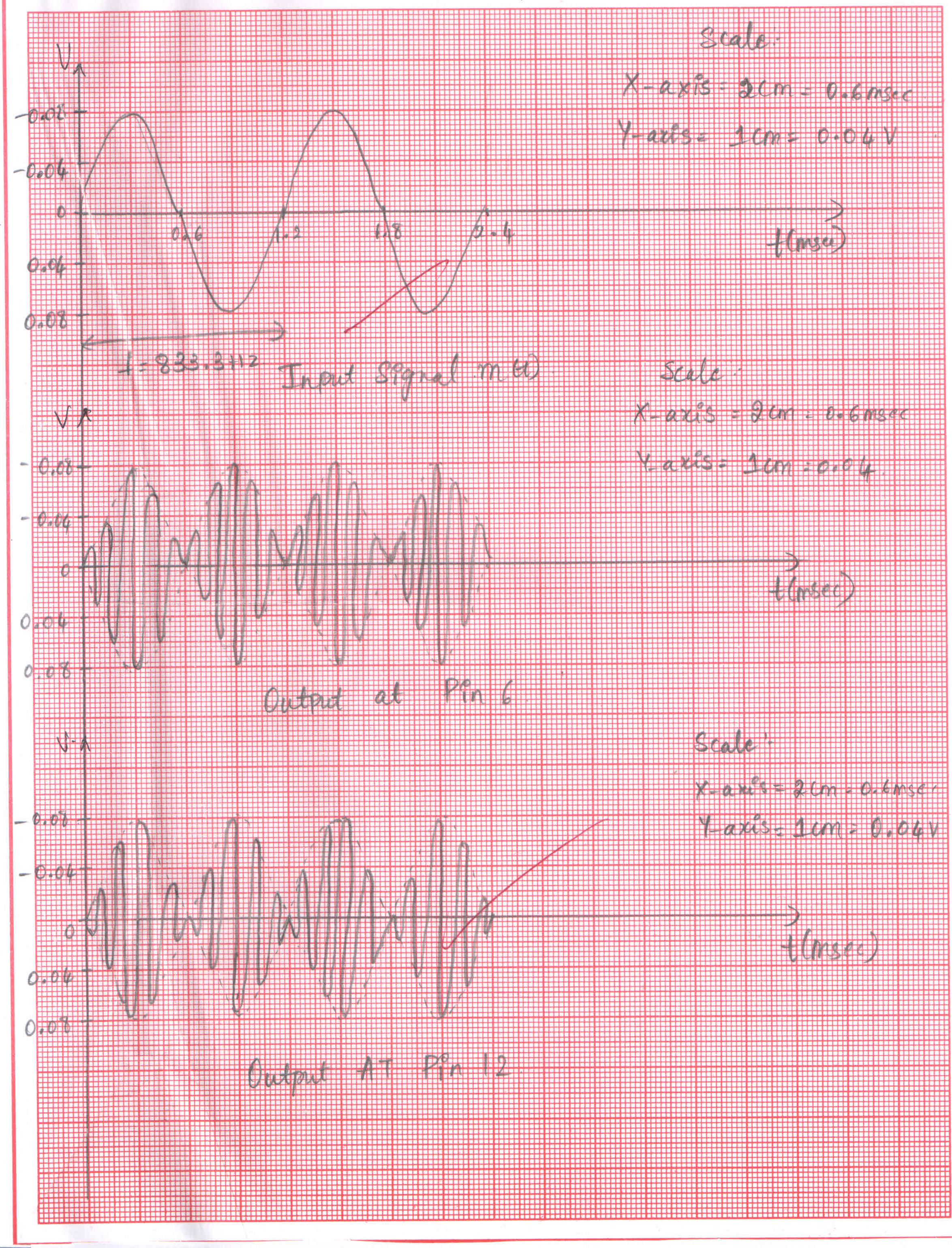
Procedure :-

1. Make the connections as shown in circuit diagram.
2. Apply +12V & -12V to the IC 8038 as supply voltage

Output Waveform.



DATE


Scale:
X-axis = 2cm = 0.6msec
Y-axis = 1cm = 0.04 V
V
0.02
0.04
0
0.6
1.2
1.8
2.4
t(msec)
0.04
0.08
t = 833.3 μs
Input Signal m(t)
Scale:
X-axis = 2cm = 0.6msec
Y-axis = 1cm = 0.04
V
0.08
0.04
0
0.04
0.08
t(msec)
Output at Pin 6
Scale:
X-axis = 2cm = 0.6msec
Y-axis = 1cm = 0.04V
V
0.08
0.04
0
0.04
0.08
t(msec)
Output AT Pin 12

from regulated power supply.

3. Set the carrier wave amplitude and frequencies and also the modulating signal amplitude and frequencies so as to get the DSBSC wave.

4 - Check for the positive and negative output voltage at pin no. 6 & 12 with respect to ground.

5. Observe the phase reversals at the cross point.

Result :-

DSBSC signal is generated using Balanced Modulator IC 1496.

	Marks Obtained
Observation (10)	08
Record (10)	08
Viva (5)	03
Total (25)	19

15/5/19

Kammavari Sangham (R)-1952

K.S.GROUP OF INSTITUTIONS

K.S. INSTITUTE OF TECHNOLOGY

(Approved by AICTE & Affiliated to VTU)

KANAKAPURA ROAD, BANGALORE - 560 062

I A, PRACTICAL TEST /PROJECT VIVA- VOCE

Course/Branch: Electronics & Communication

1	k	s	1	7	E	C	0	3	2

University Seat Number

Subject: LIC LAB

Subject Code: 17ECL48

Total number of supplements tied together : 1 + _____ = _____

Date: 10 04 2019 (D D M M Y Y Y Y)

Deepani. G

Signature of the Candidate

Entries to be made by the examiners

SCHEME OF AWARDING MARKS

Practical Examination			Project viva -voce		
a.	Procedure & write up	: of Max. Marks	a. Project Work	:	40% of Max .Marks
b.	Conducting the practicals, calculations, graphs, results, etc.,	: of Max. Marks	b. Presentation	:	30% of Max .Marks
c.	Viva-voce	: of Max. Marks	c. Viva-voce	:	30% of Max .Marks

Question Number	Marks awarded			
	a 15	b 70	c 15	Total
1	40	65	15	90/100
2				
3				
4				

14

15

Title of the Project				
Total Max Marks	Marks awarded			
	a	b	c	Total

Total Maximum Marks :	100	Total Marks obtained :	90
Marks awarded in words :	ZERO	NINE	ZERO

Total Marks obtained : _____

Marks awarded in words : _____

Examiner 1	Examiner 2
Name : Ramya 10/04/19	_____
Signature with Date : _____	_____

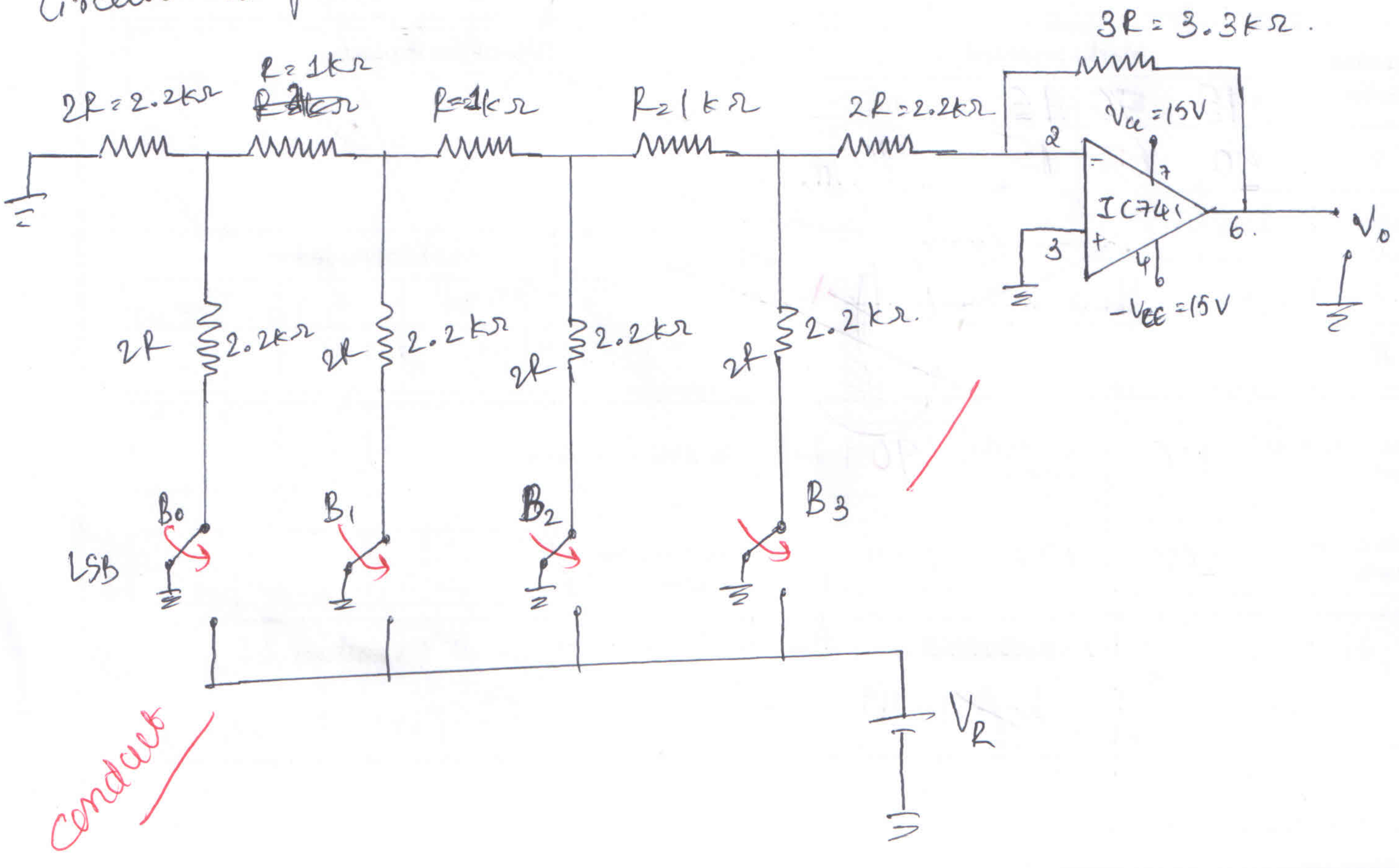
05 Q). Conduct an experiment to verify the output of a 4-bit ~~R-R~~ R-2R Converter using mod-16 Counter.

Aim:- To verify the output of a 4-bit R-2R converter using mod-16 counter.

Apparatus:-

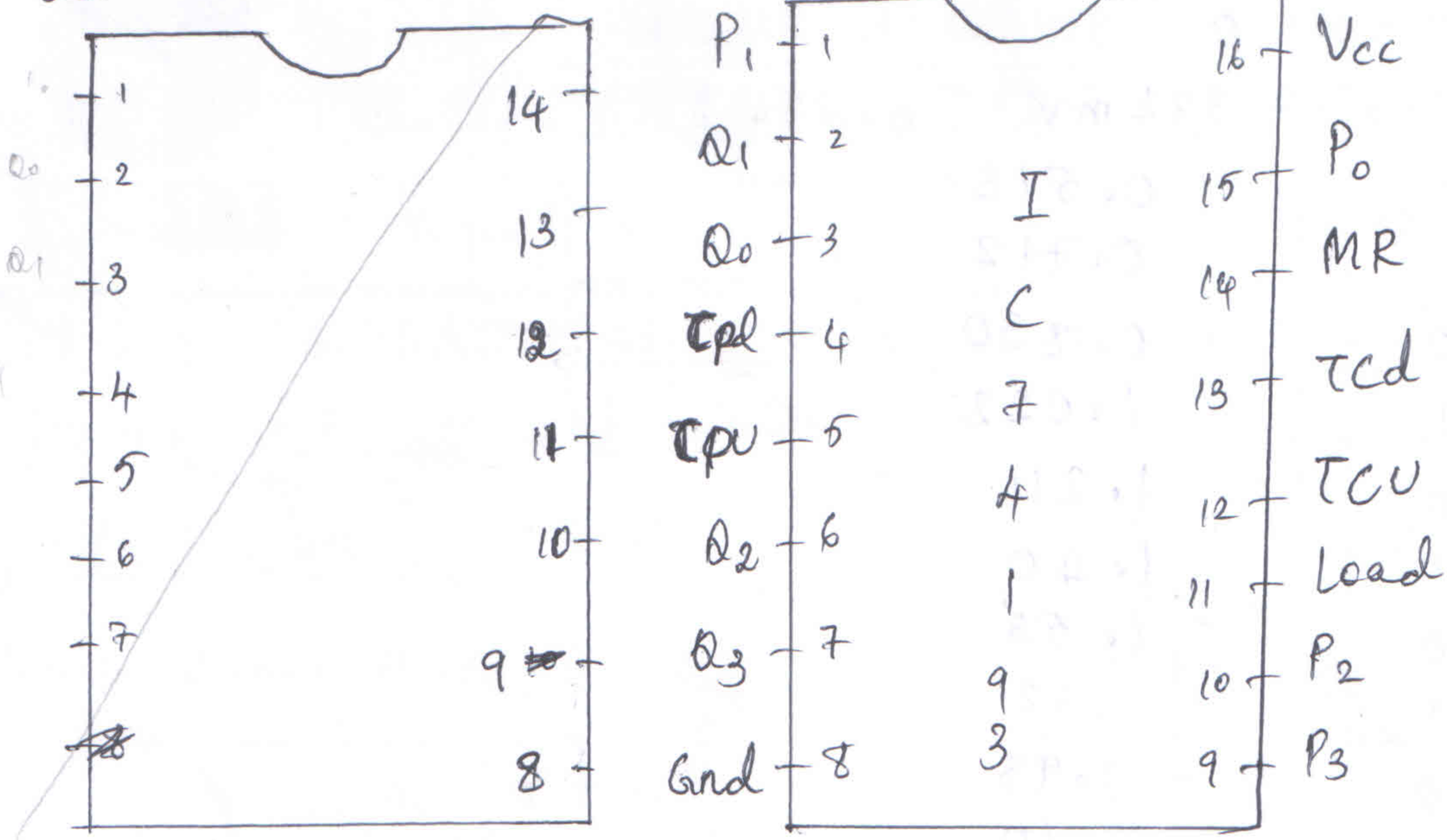
SI. No	Components	Quantity
1	Regulated power supply ±15V	1
2.	Function gen.	1
2.	CRO	1
3.	IC741	
4.	Resistors :-	
	3.3 kΩ.	1
	2.2kΩ.	6
	1kΩ.	3
5.	Multimeter	1
6.	Bread board, Connecting Wires.	1 set

Circuit diagram:-



IC74193.

Pin-details.



B.

Pin details	discriptions.
P0 - P3	Parallel input data.
Q0 - Q3	Output.
MR	Master reset (clr)
Load	Asynchronous ~~loa~~ parallel load (active high)

IC74193 as Up/down Counter. Truth table.

Clock	Q_3	Q_2	Q_1	Q_0
↓	0	0	0	0
↓	0	0	0	1
↓	0	0	1	0
↓	0	0	1	1
↓	0	1	0	0
↓	0	1	0	1
↓	0	1	1	0
↓	0	1	1	1
↓	1	0	0	0
↓	1	0	0	1
↓	1	0	1	0
↓	1	0	1	1
↓	1	1	0	0
↓	1	1	0	1
↓	1	1	1	0

Binary Inputs B_3 B_2 B_1 B_0	Analog output voltag V_o.
0 0 0 0	0
0 0 0 1	- 334mv = 0.334
0 0 1 0	- 0.518
0 0 1 1	- 0.712
0 1 0 0	- 0.830
0 1 0 1	- 1.022
0 1 1 0	- 1.211
0 1 1 1	- 1.40
1 0 0 0	- 1.53
1 0 0 1	- 1.72
1 0 1 0	- 1.98
1 0 1 1	- 2.10
1 1 0 0	- 2.21
1 1 0 1	- 2.40
1 1 1 0	- 2.59
1 1 1 1	- 2.781

o/p

Result :-

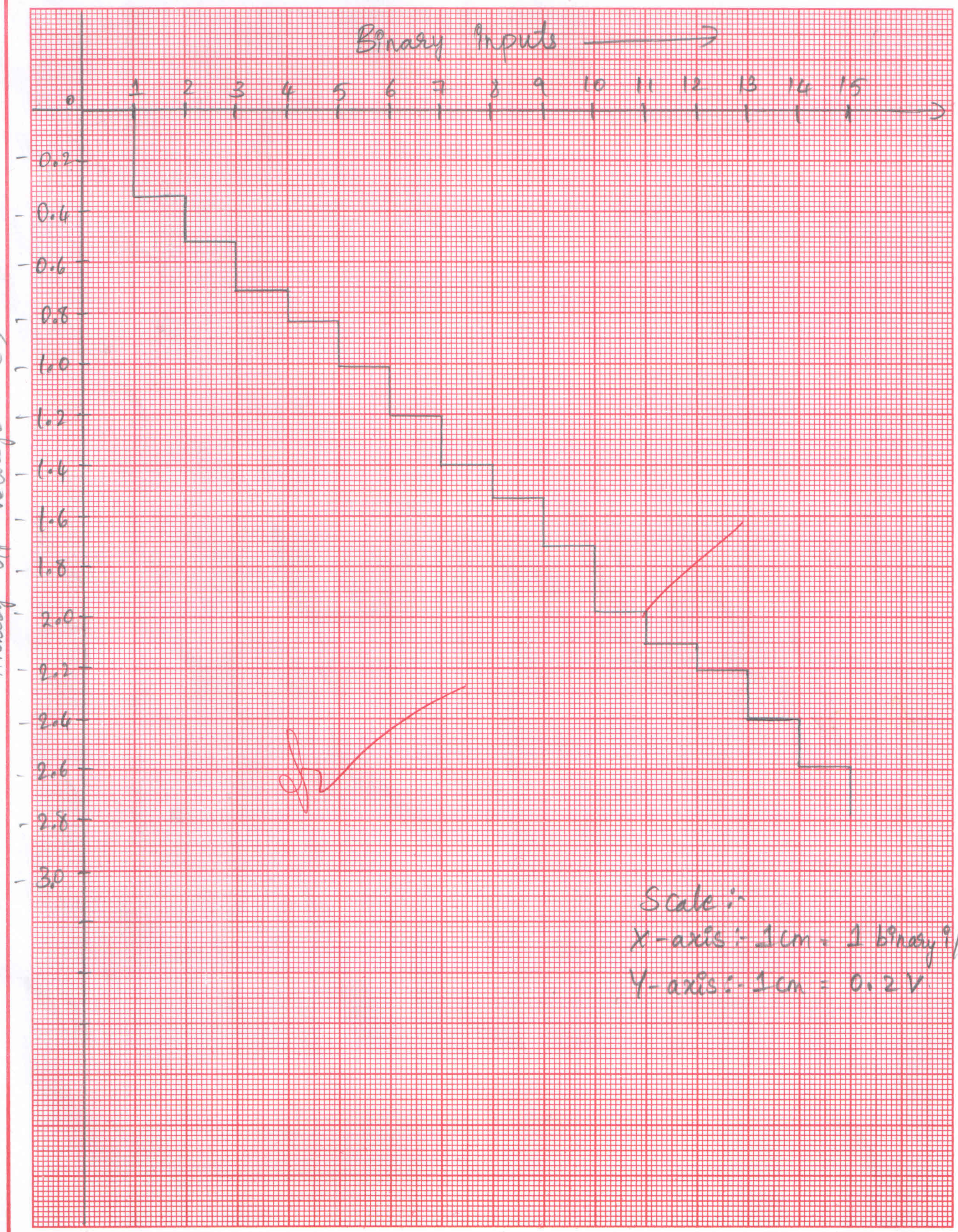
Full scale o/p voltage	Theoretical output voltage (Full scale)	Practical output voltage using mod 16-counter (Full scale)
5V.	5V.	- 2.781 V.

The output of a 4-bit R-2R Converter using mod-16 Counter is verified.

USN: 1KS17EC032

Name: DEVYANI.G

Date: 10/04/2019



Chandra's

Kammavari Sangham (R)-1952

K.S.GROUP OF INSTITUTIONS

K.S. INSTITUTE OF TECHNOLOGY

(Approved by AICTE & Affiliated to VTU)

KANAKAPURA ROAD, BANGALORE - 560 062

I A, PRACTICAL TEST /PROJECT VIVA- VOCE

Course/Branch: Electronics & Communication

1	k	8	1	7	E	C	0	3	2

University Seat Number

Subject: Linear IC's & Communication Lab Subject Code: 17ECL48

Total number of supplements tied together : 1 + _____ = _____

Date: 14 05 2019 (DD MM YYYY)

Deepyani. b

Signature of the Candidate

Entries to be made by the examiners

SCHEME OF AWARDING MARKS

Practical Examination			Project viva -voce		
a.	Procedure & write up	: of Max. Marks	a.	Project Work	: 40% of Max .Marks
b.	Conducting the practicals, calculations, graphs, results, etc.,	: of Max. Marks	b.	Presentation	: 30% of Max .Marks
c.	Viva-voce	: of Max. Marks	c.	Viva-voce	: 30% of Max .Marks

Question Number	Marks awarded			
	a	b	c	Total
1	08	50	07	065
2				10
3				
4				15

Title of the Project				
Total Max Marks	Marks awarded			
	a	b	c	Total

Total Maximum Marks :	100	Total Marks obtained :	085	
Marks awarded in words :	Zero	Six	Five	

Total Marks obtained :

Marks awarded in words :

Examiner 1

Examiner 2

Name : Ayesha 14/5/19

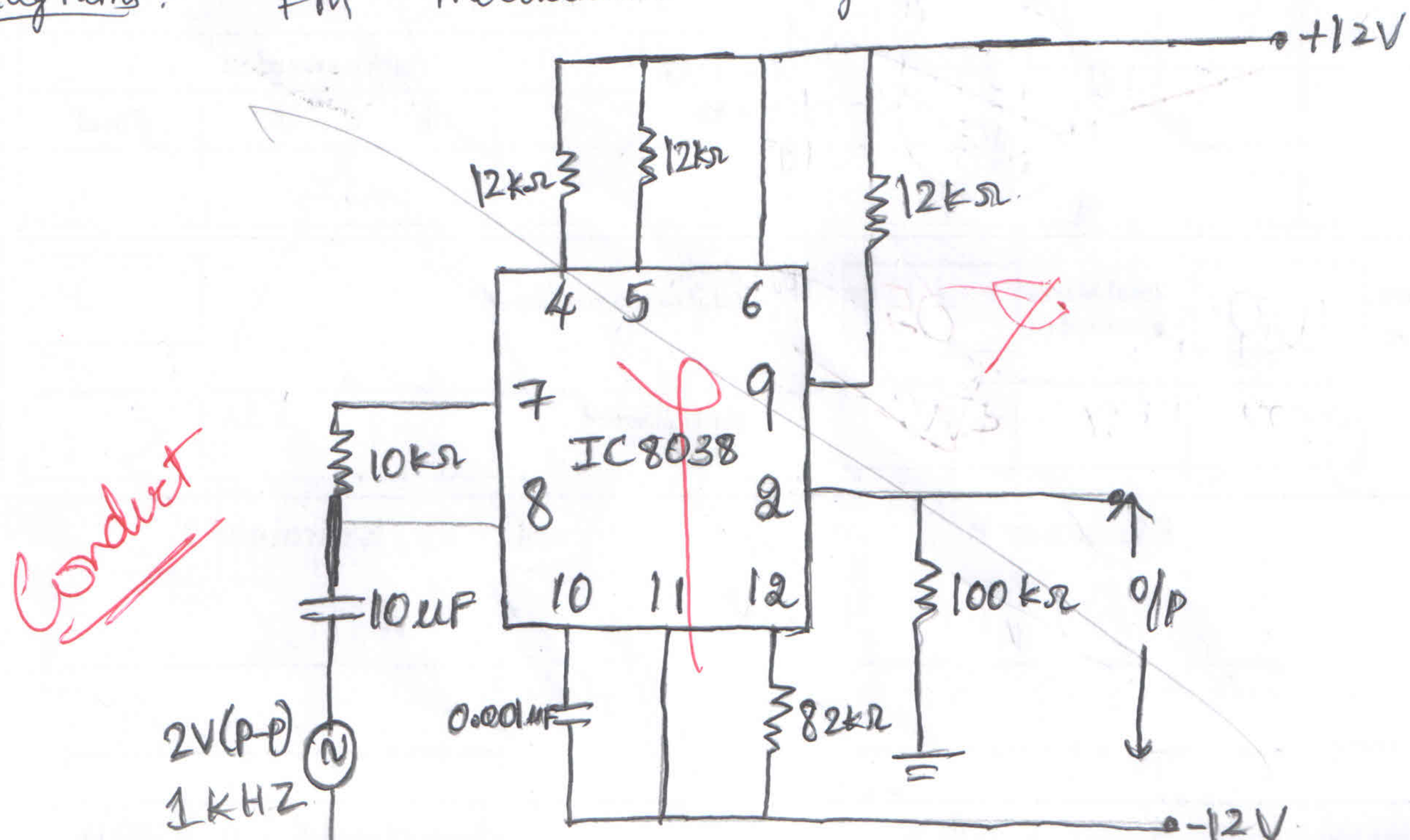
Signature with Date : _____

Aim :- Conduct an experiment to generate Amplitude modulated signal to measure modulation index and also perform the demodulation to get modulating signal.

Components Required :-

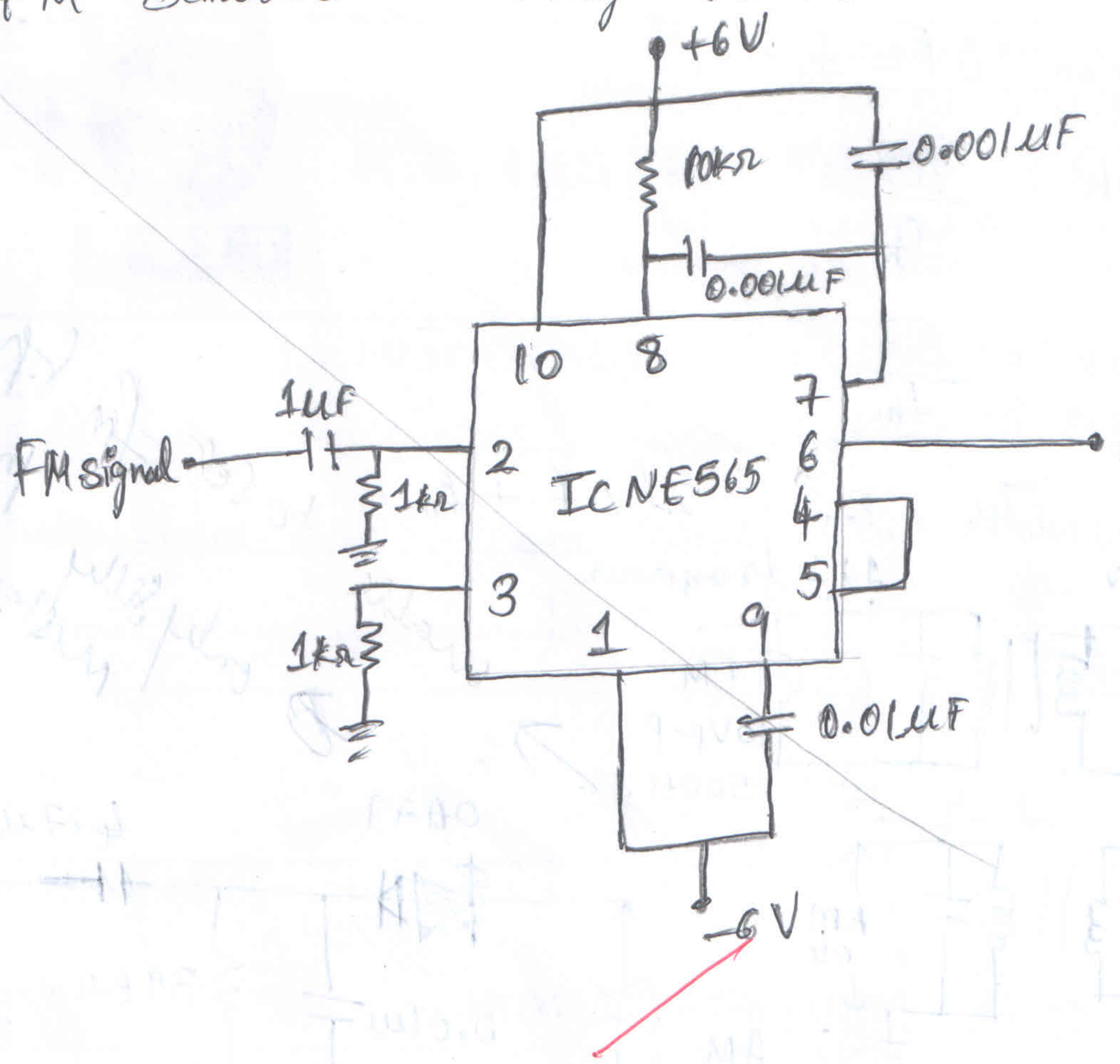
SI.NO.	Components	Quantity.
1.	Regulated power supply ±12V.	1
2.	~~Regulated power supply ± 6V~~	1
3.	Function generator	1
4.	CRO	1
5.	Transistor 8400	~~Each~~ 1
6	~~IC8038~~, ~~ICNE565~~ IFT 455kHz	1
7.	1:1 transformer	1
	Resistors.	
	~~12 kΩ~~ 100kΩ	1 ~~3~~
	~~82kΩ~~ 10Ω	1 ~~4~~
	~~100 kΩ~~ 39kΩ	1 ~~2~~
	~~10 kΩ~~	~~2~~
	~~1 kΩ~~	1 ~~2~~
8	OA79 diode	3
9.	Capacitors :- 0.01μF	
	~~0.001 μF, 0.01μF, 10μF, 1μF~~ 4.7μF	~~Each~~ 1.
10.	Bread board, Connecting Wires	1 Set

Diagrams :- FM Modulation Using IC8038



Conduct

FM Demodulation Using IC NE565.



Waveforms:-

Calculations :-

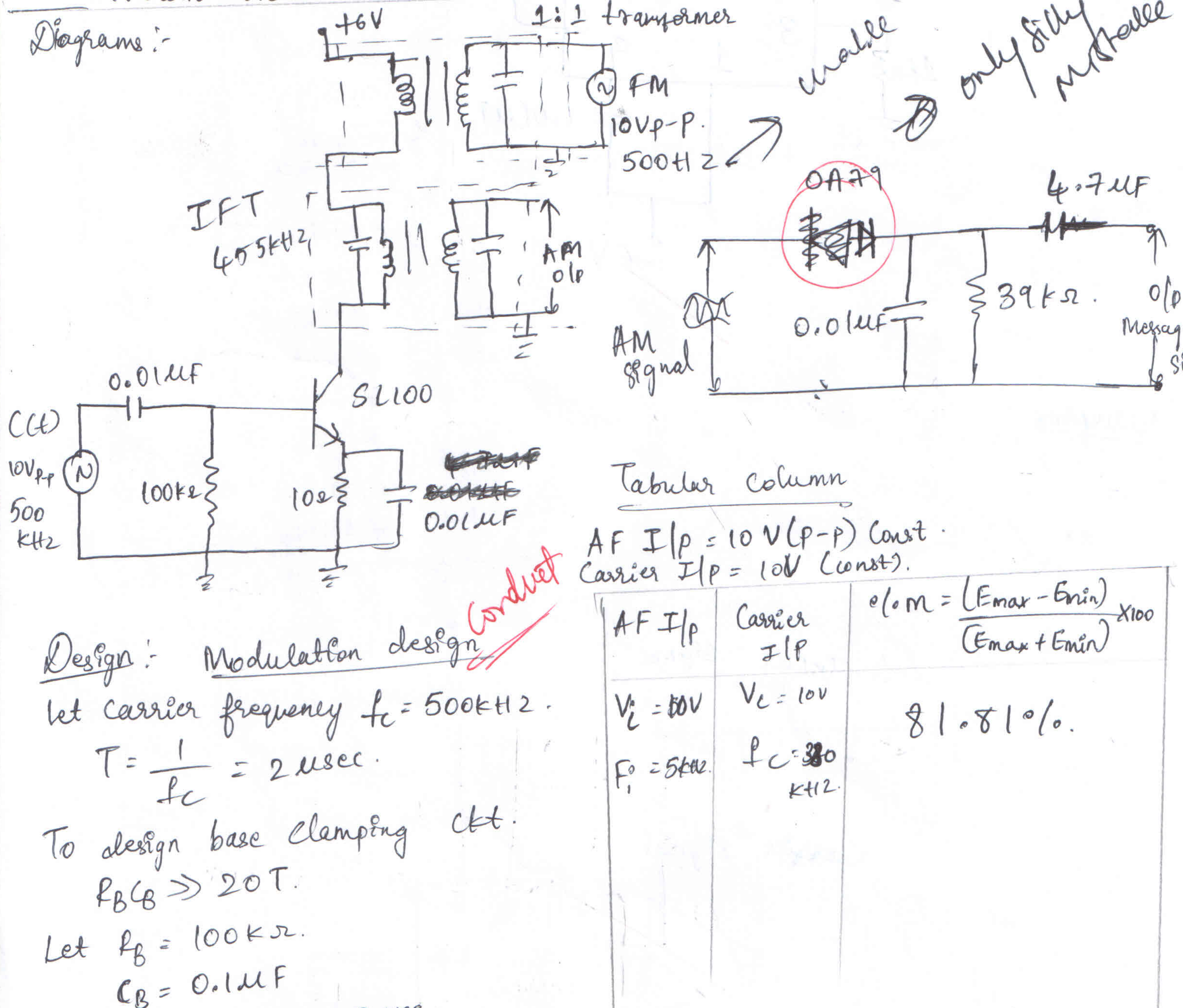
Frequency deviation, $\Delta f = f_2 - f_1$

~~Bandwidth, B.W = $\frac{\Delta f}{f_m}$~~

Modulation index = $\frac{\Delta f}{f_m}$

Transmission Bandwidth, $B_T = 2(\Delta f + f_m)$ to set fm signal property

Diagrams :-



Tabular Column

AF I/p = 10 V(p-p) Const.
Carrier I/p = 10V (const).

AF I/p	Carrier I/p	$\%m = \frac{(E_{max} - E_{min})}{(E_{max} + E_{min})} \times 100$
$V_i = 10V$	$V_c = 10V$	81.81%.
$F_i = 5kHz$.	$f_c = 330$ kHz.	

$V_{max} = 2 \times 10 = 20$ V.

$V_{min} = 0.2 \times 10 = 2$ V.

Design :- Modulation design (conduct)

let carrier frequency $f_c = 500kHz$.

$T = \frac{1}{f_c} = 2\mu sec$.

To design base clamping ckt.

$R_B C_B \gg 20T$.

Let $R_B = 100k\Omega$.

$C_B = 0.1\mu F$

$1000\mu sec \gg 20 \times 2\mu sec$.

$1000\mu sec \gg 40\mu sec$.

Demodulation design

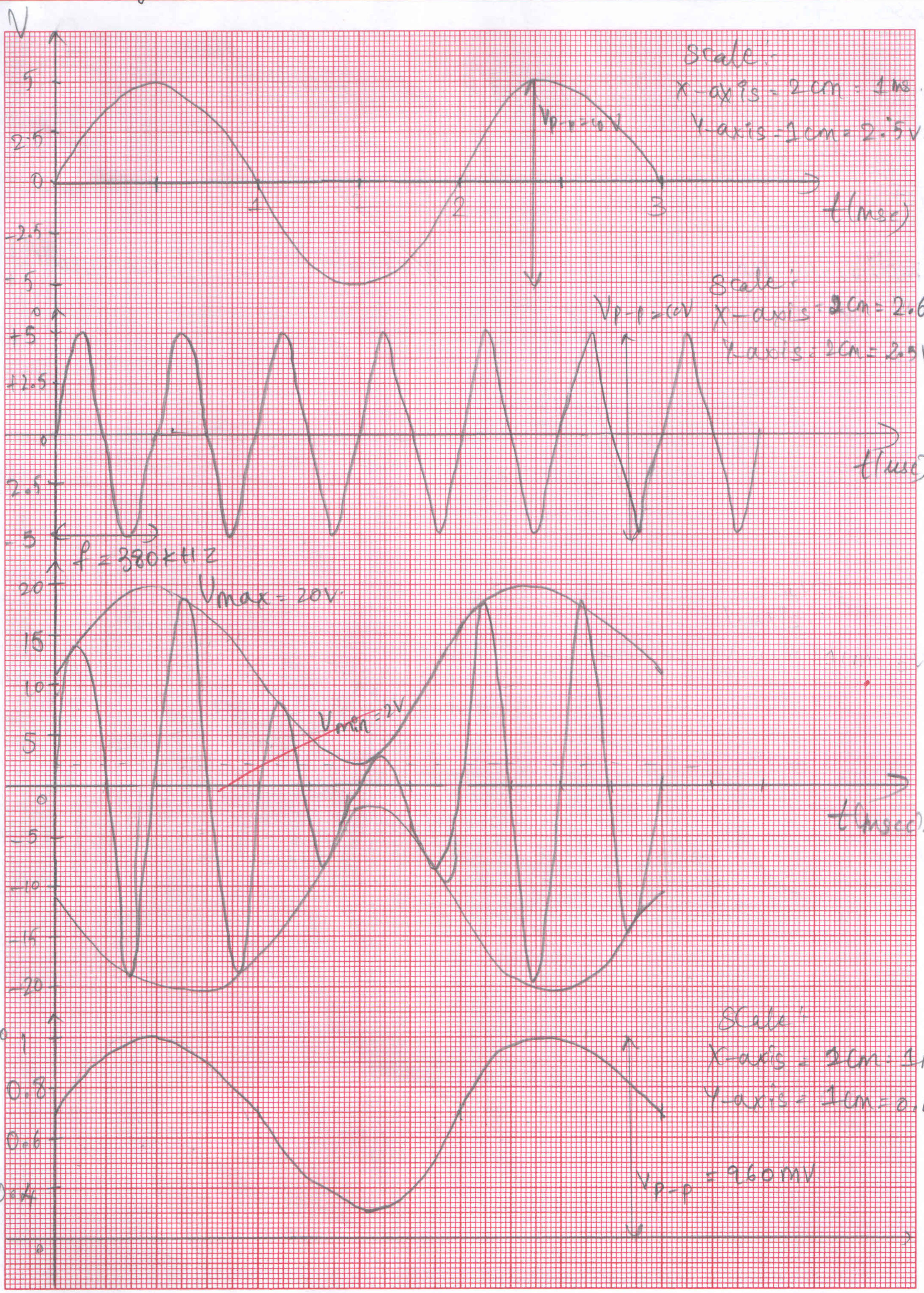
$\frac{1}{f_m} \gg RC \gg \frac{1}{f_c}$.

; $R = 39k\Omega$, $C = 0.01\mu F$.

let $RC \gg \frac{20}{f_c}$ =>

let $f_c = 455kHz$, $f_m = 500Hz$.

Name... Deviyani. G. Date.....



Visvesvaraya Technological University

K.S. INSTITUTE OF TECHNOLOGY BENGALURU

Branch : EC Scheme : 2017 Semester : 4

Sl NO.	USN	17CPH49	17EC42	17EC43	17EC44	17EC45	17EC46	17ECL47	17ECL48	17MAT41	STUDENT SIGNATURE
1	1KS16EC001	15	20	19	19	20	21	26	20	22	
2	1KS16EC038	-	27	19	23	21	22	32	32	31	
3	1KS16EC068	15	26	22	31	28	27	28	32	27	
4	1KS16EC086	-	40	35	37	34	35	40	36	39	
5	1KS16EC113	15	19	19	21	20	19	20	22	23	
6	1KS17EC001	16	34	35	34	32	32	34	37	36	
7	1KS17EC002	15	29	26	31	28	34	35	36	30	
8	1KS17EC003	17	31	31	34	35	30	38	36	30	
9	1KS17EC004	15	30	26	31	32	29	37	33	33	
10	1KS17EC005	16	26	27	31	28	26	28	35	28	
11	1KS17EC006	16	27	28	35	32	27	34	35	34	
12	1KS17EC007	17	25	28	30	26	30	33	33	30	
13	1KS17EC008	16	26	23	29	29	20	35	34	27	
14	1KS17EC009	15	39	33	39	38	35	39	35	38	
15	1KS17EC010	16	30	25	30	30	29	35	34	28	
16	1KS17EC011	16	30	27	32	26	29	33	31	29	
17	1KS17EC012	17	33	27	37	35	28	34	34	33	
18	1KS17EC013	15	31	27	34	33	30	37	33	33	
19	1KS17EC014	17	36	31	36	35	29	40	35	38	
20	1KS17EC015	15	40	35	39	38	36	39	37	39	
21	1KS17EC016	15	27	28	37	28	29	37	30	33	
22	1KS17EC017	15	27	24	30	24	24	33	32	26	
23	1KS17EC018	17	30	26	34	32	29	33	34	33	
24	1KS17EC019	18	30	32	26	31	26	39	35	33	
25	1KS17EC020	16	39	30	39	34	31	36	33	40	
26	1KS17EC021	16	32	26	34	31	28	35	32	34	
27	1KS17EC022	15	31	31	35	29	32	37	35	36	
28	1KS17EC023	15	33	29	35	29	30	35	32	28	
29	1KS17EC024	15	36	27	38	32	31	37	32	36	
30	1KS17EC025	15	38	36	36	36	35	38	36	36	
31	1KS17EC026	15	27	20	25	20	20	31	20	28	
32	1KS17EC027	15	25	21	26	23	24	35	25	27	
33	1KS17EC028	17	39	34	40	36	31	40	36	38	
34	1KS17EC029	17	26	34	32	30	28	37	33	34	
35	1KS17EC030	15	36	31	32	28	25	36	36	37	
36	1KS17EC031	15	35	32	31	31	27	37	35	38	
37	1KS17EC032	15	37	32	35	37	38	40	34	36	
38	1KS17EC033	15	27	28	28	28	23	34	32	33	
39	1KS17EC035	16	24	31	34	25	36	33	37	26	
40	1KS17EC036	15	31	34	36	36	34	38	37	38	
41	1KS17EC037	15	19	20	22	19	23	22	26	21	

Sl NO.	USN	17CPH49	17EC42	17EC43	17EC44	17EC45	17EC46	17ECL47	17ECL48	17MAT41	STUDENT SIGNATURE
42	1KS17EC038	15	22	26	35	34	29	31	30	34	
43	1KS17EC039	15	27	32	39	33	29	33	34	39	
44	1KS17EC040	16	33	32	39	36	33	39	35	38	
45	1KS17EC041	17	23	26	37	30	32	38	36	29	
46	1KS17EC042	16	22	25	31	25	22	30	29	28	
47	1KS17EC043	15	28	25	34	33	34	27	30	29	
48	1KS17EC044	17	25	31	32	31	31	34	35	32	Sushma
49	1KS17EC045	17	35	40	38	40	36	39	39	40	
50	1KS17EC046	16	19	32	34	29	30	34	35	30	
51	1KS17EC047	16	22	29	32	35	33	32	35	32	
52	1KS17EC048	16	22	31	31	28	32	36	37	39	
53	1KS17EC049	16	21	34	34	32	27	35	37	33	M.Ranjith
54	1KS17EC050	16	40	40	40	40	38	39	39	40	
55	1KS17EC051	17	35	36	40	35	37	33	37	35	
56	1KS17EC052	15	31	31	39	32	29	32	37	36	
57	1KS17EC053	16	22	24	30	26	22	28	29	29	
58	1KS17EC054	14	19	20	22	19	22	22	26	21	
59	1KS17EC055	15	20	29	30	31	29	31	35	32	
60	1KS17EC056	15	28	32	35	26	27	36	37	39	
61	1KS17EC057	15	27	26	29	31	27	34	35	30	
62	1KS17EC058	15	19	26	29	33	25	31	33	28	
63	1KS17EC059	16	24	32	35	34	33	34	36	33	
64	1KS17EC060	16	24	30	33	33	28	31	29	33	
65	1KS17EC061	14	19	28	30	27	25	27	29	35	
66	1KS17EC062	15	29	36	35	32	28	34	37	40	
67	1KS17EC063	15	24	33	34	34	31	35	37	36	
68	1KS17EC064	15	19	26	28	26	26	28	32	34	
69	1KS17EC065	14	19	26	30	35	21	28	34	33	
70	1KS17EC066	16	29	36	38	36	34	38	37	37	
71	1KS17EC067	16	35	34	38	36	34	33	38	40	
72	1KS17EC068	16	30	28	38	37	33	39	37	40	
73	1KS17EC069	16	22	25	29	27	26	26	32	32	
74	1KS17EC070	14	21	23	28	19	24	23	25	22	
75	1KS17EC071	16	30	33	38	35	35	38	36	38	
76	1KS17EC072	17	30	34	35	36	32	38	37	39	
77	1KS17EC073	17	28	24	31	27	27	32	35	28	
78	1KS17EC074	16	21	19	20	21	21	26	33	25	
79	1KS17EC075	17	40	38	40	40	33	38	40	40	
80	1KS17EC076	18	38	31	37	40	27	36	39	40	
81	1KS17EC077	16	24	19	25	29	21	27	34	28	
82	1KS17EC078	16	34	34	37	33	30	33	34	33	
83	1KS17EC079	16	34	37	33	33	29	34	36	35	
84	1KS17EC080	16	34	27	29	38	26	37	38	33	
85	1KS17EC082	14	23	19	29	36	22	32	34	26	
86	1KS17EC083	16	20	20	22	22	20	28	33	27	
87	1KS17EC084	16	34	27	36	34	25	34	36	37	
88	1KS17EC085	17	28	33	40	39	35	33	39	39	
89	1KS17EC086	13	23	22	23	32	21	31	34	33	
90	1KS17EC087	16	21	19	28	23	22	30	31	29	
91	1KS17EC088	16	24	26	34	35	27	32	35	29	

Sl NO.	USN	17CPH49	17EC42	17EC43	17EC44	17EC45	17EC46	17ECL47	17ECL48	17MAT41	STUDENT SIGNATURE
92	1KS17EC089	17	20	19	26	32	21	29	35	30	
93	1KS17EC090	16	35	36	38	37	29	38	38	37	
94	1KS17EC092	16	36	33	32	38	28	36	37	38	
95	1KS17EC093	15	33	32	35	36	28	37	36	34	
96	1KS17EC094	15	31	34	36	34	27	37	40	34	
97	1KS17EC095	16	23	21	33	33	25	32	36	32	
98	1KS17EC096	15	33	29	34	38	28	34	36	36	
99	1KS17EC097	15	39	31	36	37	30	38	38	36	
100	1KS17EC098	16	32	21	36	31	24	37	37	34	
101	1KS17EC099	14	25	23	33	36	25	36	37	35	
102	1KS17EC100	16	36	28	35	35	31	34	39	38	
103	1KS17EC101	16	23	20	30	25	21	33	37	29	
104	1KS17EC102	17	31	27	36	38	25	33	38	37	
105	1KS17EC103	16	38	33	35	37	25	34	39	36	
106	1KS17EC104	15	31	26	34	35	27	36	38	38	
107	1KS17EC105	15	36	36	37	39	26	39	39	36	
108	1KS18EC401	14	19	15	19	19	20	22	28	20	
109	1KS18EC402	15	20	19	23	26	28	29	36	20	
110	1KS18EC403	15	22	23	30	29	25	32	36	25	
111	1KS18EC404	14	20	7	05	19	20	22	22	20	
112	1KS18EC405	14	20	13	19	22	19	28	34	20	
113	1KS18EC406	15	20	22	23	24	21	31	35	29	
114	1KS18EC408	15	25	19	31	30	30	34	34	27	
--x--	Faculty Signature										----xxxxxxx----

* - values are either optional subjects or the faculty has not yet entered the marks

HOD
Seal and Signature
HEAD OF THE DEPARTMENT
Dept. of Electronics & Communication Engg
K.S. Institute of Technology
Bengaluru - 560 109

PRINCIPAL
Seal and Signature
PRINCIPAL
K.S. INSTITUTE OF TECHNOLOGY
BENGALURU - 560 109