K S INSTITUTE OF TECHNOLOGY, BANGLORE
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE FILE

NAME OF THE STAFF	**: Mr. Sunil Kumar G R**
SUBJECT CODE/NAME	**: 18EC46- Microcontroller**
SEMESTER/YEAR	**: IV/II**
ACADEMIC YEAR	**: 2020 – 2021, Even**
BRANCH	**: ECE 'A'**

Course In-Charge **Module Coordinator** **HOD-ECE**

K. S. INSTITUTE OF TECHNOLOGY

VISION

"To impart quality technical education with ethical values, employable skills and research to achieve excellence".

MISSION

- To attract and retain highly qualified, experienced & committed faculty.
- To create relevant infrastructure.
- Network with industry & premier institutions to encourage emergence of new ideas by providing research & development facilities to strive for academic excellence.
- To inculcate the professional & ethical values among young students with employable skills & knowledge acquired to transform the society.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

VISION

"To achieve excellence in academics and research in Electronics & Communication Engineering to meet societal need".

MISSION

- To impart quality technical education with the relevant technologies to produce industry ready engineers with ethical values.
- To enrich experiential learning through active involvement in professional clubs & societies.
- To promote industry-institute collaborations for research & development.

K.S. INSTITUTE OF TECHNOLOGY
Department: Electronics and Communication Engg.

PROGRAM EDUCATIONAL OBJECTIVES (PEO'S)

- Excel in professional career by acquiring domain knowledge.
- Motivation to pursue higher Education & research by adopting technological innovations by continuous learning through professional bodies and clubs.
- To inculcate effective communication skills, team work, ethics and leadership qualities.

PROGRAM SPECIFIC OUTCOMES (PSO'S)

PSO1: Graduate should be able to understand the fundamentals in the field of Electronics & Communication and apply the same to various areas like Signal processing, embedded systems, Communication & Semiconductor technology.

PSO2: Graduate will demonstrate the ability to design, develop solutions for Problems in Electronics & Communication Engineering using hardware and software tools with social concerns.

K S INSTITUTE OF TECHNOLOGY

PROGRAM OUTCOMES (PO'S)

Engineering Graduates will be able to:

PO1 :Engineering knowledge: Apply the knowledge of mathematics, science, engineeringfundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 : Problem analysis: Identify, formulate, review research literature, and analyze complexengineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 : Design/development of solutions: Design solutions for complex engineering problems anddesign system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 : Conduct investigations of complex problems: Use research-based knowledge and researchmethods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 : Modern tool usage: Create, select, and apply appropriate techniques, resources, and modernengineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6 : The engineer and society: Apply reasoning informed by the contextual knowledge to assesssocietal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 : Environment and sustainability: Understand the impact of the professional engineering solutionsin societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 : Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms ofthe engineering practice.

PO9 :Individual and team work: Function effectively as an individual, and as a member or leader indiverse teams, and in multidisciplinary settings.

PO10 :Communication: Communicate effectively on complex engineering activities with the engineeringcommunity and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 ;Project management and finance: Demonstrate knowledge and understanding of theengineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage inindependent and life-long learning in the broadest context of technological change.

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#14, Raghuvanahalli, Kanakapura Main Road, Bengaluru-5600109

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CO, PO and PSO Mapping

Course: Microcontroller			
Course In charge: Mr. Sunil Kumar G.R.			
Type: Open Elective		**Course Code:18EC46**	
No of Hours per week			
Theory (Lecture Class)	Practical/Field Work/Allied Activities	Total/Week	Total teaching hours
4	0	4	46
Marks			
Internal Assessment	Examination	Total	Credits
40	60	100	3

Aim/Objective of the Course:

This course enables students to:

- Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers.
- Familiarize the basic architecture of 8051 microcontroller.
- Program 8051microprocessor using Assembly Level Language and C.
- Understand the interrupt system of 8051 and the use of interrupts.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051.
- Interface 8051 to external memory and I/O devices using its I/O ports.

Course Learning Outcomes:

After completing the course, the students will be able to,

		Bloom's Level
CO1	Distinguish the role of functional units in the architecture of 8051 microcontroller	K2 understanding
CO2	Identify various instructions of 8051 Microcontroller	K3 Applying
CO3	Build solutions using assembly level language and high level language	K3 Applying
CO4	Make use of timers/counters, serial port and interrupts to generate delay and perform serial communication	K3 Applying
CO5	Design interfacing of peripherals to 8051 Microcontroller	K4 Analyzing

Syllabus Content:

Module1: 8051 Microcontroller: Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing LO: At the end of this session the student will be able to, 1. Understand the difference between Microprocessor and Microcontroller 2. Understand Architecture of Microcontroller 8051 3. Understand how memory can be interfaced to Microcontroller	**CO1** **08 hrs** PO1-3 PO2-1 P10-2
Module 2:	**CO2**

8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, and Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions. LO: At the end of this session the student will be able to, 1.Understand the classification of instruction set 2. Understand the working of instruction set 3. Able to write small programs using the instructions	**08h hrs** PO1-3 PO2-2 PO5-2
Module 3: 8051 Stack, I/O Port Interfacing and Programming: 8051 Stack, Stack and Subroutine instructions. Assembly language program examples on subroutine and involving loops - Delay subroutine, Factorial of an 8 bit number (result maximum 8 bit), Block move without overlap, Addition of N 8 bit numbers, Picking smallest/largest of N 8 bit numbers. Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status LO: At the end of this session the student will be able to, **1.** Understand the need of stack in microcontroller **2.** Meaning of subroutine and how to write subroutine for different requirement **3.** Interfacing of LED and codes for controlling it	**CO3** **08 hrs** PO1-3 PO2-3 PO5-2
Module 4: 8051 Timers and Serial Port: 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin. 8051 Serial Communication- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially LO: At the end of this session the student will be able to, 1. Understand the working of timers 2. Write program for generating delay using timers 3. Understand how timer can be used as counter 4. Able to understand the working of serial communication and write program	**CO4** **8 hrs** PO1-3 PO2-3 PO5-2
Module -5: 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt. Interfacing 8051 to ADC-0804, LCD and Stepper motor and their 8051 Assembly language interfacing programming LO: At the end of this session the student will be able to, 1. Understand the interrupts present in 8051 and its working 2. Able to write the program for timers and serial communication using interrupts 3. Understand the interfacing of ADC, LCD and stepper motor and write the program for the same	**CO5** **08 hrs** PO1-3 PO2-3 PO3-3 PO5-1
Text Books: - 1. The 8051 Microcontroller and Embedded Systems – using assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006. 2. "The 8051 Microcontroller", Kenneth J. Ayala, 3rd Edition, Thomson/Cengage Learning.	
Reference Books: 1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4. 2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.	
Useful Journals: Journal of Microcontroller Engineering and Applications Journals.elsevier.com › microprocessors-and-microsystems	

Journal of Microcontroller Engineering and Applications

Teaching and Learning Methods:

1. Lecture class: 47 hrs.
2. Self-study: 5hrs.
3. Field visits/Group Discussions/Seminars: 03hrs.

Assessment:

Type of test/examination: Written examination

Continuous Internal Evaluation(CIE) : 40 marks

Semester End Exam(SEE) : 60 marks (students have to answer all main questions)

Test duration: 1 :30 hr

Examination duration: 3 hrs

CO - PO MAPPING

PO1: Science and engineering Knowledge **PO2:** Problem Analysis **PO3:** Design & Development **PO4:**Investigations of Complex Problems **PO5:** Modern Tool Usage **PO6:** Engineer & Society	**PO7:**Environment and Society **PO8:**Ethics **PO9:**Individual & Team Work **PO10:** Communication **PO11:**Project Mngmt & Finance **PO12:**Life long Learning

PSO1: Graduate should be able to understand the fundamentals in the field of Electronics & Communication and apply the same to various areas like Signal processing, embedded systems, Communication & Semiconductor technology.

PSO2: Graduate will demonstrate the ability to design, develop solutions for Problems in Electronics & Communication Engineering using hardware and software tools with social concerns.

CO 15EC563	Bloom's Level	PO1	PO2	P03	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2
CO1	K2	3	1	-	-	-	-	-	-	-	2	-	-	3	3
CO2	K3	3	1	-	-	2	-	-	-	-	-	-	-	3	3
CO3	K3	3	3	-		2	-	-	-	-	-	-	-	3	3
CO4	K3	3	3	-	-	2	-	-	-	-	-	-	-	3	3
CO5	K4	3	3	3	-	1	-	-	-	-	-	-	-	3	3
18EC46		3	2.2	3	-	1.8	-	-	-	-	2	-	-	3	3

Justification for CO-PO mapping

CO -Subject Code	Justification for PO mapping

CO1	PO1: Should have a strong knowledge of Digital circuits PO2: Should have the ability of solving simple problems P10: should able to write the report about mapping of memory
CO2	PO1: Should have a strong knowledge of the architecture of microcontroller to understand the instructions PO2: Should have the ability of solving simple problems PO5: Capable of using the Modern Tool for understanding the working of the instructions
CO3	PO1: Should have a strong knowledge of the of the instruction set to write the program for 8051 PO2: Should have the ability of solving simple problems PO5: Capable of using the Modern Tool for understanding the working of the program
CO4	PO1: Should have a strong knowledge of the of the instruction set to write the program for timers and serial communication PO2: Should have the ability of solving simple problems PO5: Capable of using the Modern Tool for understanding the working of the program
CO5	PO1: Should have a strong knowledge of the of the programming to write the program PO2: Should have the ability of solving simple problems PO3: Should have the strong knowledge of Designing so that interfacing of ADC and LCD can be understood for using it for the required applications PO5: Capable of using the Modern Tool for understanding the working of the program

CO PO mapping for the events conducted after gap identification

Sl. No.	Gap Identification	CO	Relevant PO Mapping
1	Class test for solving Complex problems		PO4
2	Quiz		P10
3	Mini Project		PO9, PO10,PO11, PO12

Course in-Charge **Module Coordinator** **HOD**

K. S INSTITUTE OF TECHNOLOGY, BENGALURU-560109

TENTATIVE CALENDAR OF EVENTS: EVEN SEMESTER (2020-2021)

SESSION: APR 2021 - AUG2021

Week No.	Month	Day						Days	Activities
		Mon	Tue	Wed	Thu	Fri	Sat		
1	APR	19 *	20	21	22	23	24	6	19*-Commencement of Higher Semester 24 Wednersday Time Table
2	APR/MAY	26	27	28	29	30	1H	5	1 May Day
3	MAY	3	4	5	6	7	8	6	8 Monday Time Table
4	MAY	10	11	12	13H	14H	15DH	3	13 Idul Fitr 14 Basava Jayanti
5	MAY	17	18	19	20	21	22TA	6	22 Tuesday Time Table
6	MAY	24 T1	25T1	26T1	27	28	29DH	5	
7	MAY/JUN	31	1	2	3	4	5ASD	6	5 Wednersday Tme Table
8	JUN	7	8	9	10	11	12DH	5	
9	JUN	14	15	16	17	18	19	6	19 Monday Time Table
10	JUN	21	22	23	24	25TA	26DH	5	
11	JUN/JUL	28 T2	29T2	30T2	1	2	3	6	3 Thursday time Table
12	JUL	5	6	7	8	9ASD	10DH	5	
13	JUL	12	13	14	15	16	17	6	17 Tuesday Time Table
14	JUL	19 T3(VIII)	20 * T3(VIII)	21H	22	23	24DH	4	20 *VIII Sem Last working day 21 Bakrid / Eid al Adha
15	JUL	26	27	28TA	29	30	31	6	
16	AUG	2	3	4	5 T3	6 T3	7*T3	6	7 Wednersday Tme Table 7* IV &VI Last working day
		Total No of Working Days : 86							

Total Number of working days (Excluding holidays and Tests)=73

H	Holiday
T1,T2, T3	Tests 1,2, 3
ASD	Attendance & Sessional Display
DH	Declared Holiday
LT	Lab Test
TA	Test attendance

Monday	15
Tuesday	15
Wednesday	15
Thursday	14
Friday	14
Total	73

PRINCIPAL
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BENGALURU - 560 109.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

TENTATIVE CALENDAR OF EVENTS: EVEN SEMESTER (2020-2021)

SESSION: APR 2021 - AUG2021

Week No.	Month	Day						Days	Activities	Department Activities Tentative Dates
		Mon	Tue	Wed	Thu	Fri	Sat			
1	APR	19 *	20	21	22	23	24	6	19*-Commencement of Higher Semester 24 Wednesday Time Table	
2	APR/MAY	26	27	28	29	30		5	1 May Day	
3	MAY		4	5	6	7	8	6	8 Monday Time Table	3rd - 8th May AICTE - ISTE Induction / Refresher programme (FDP)
4	MAY	10	11	12			15DH	3	13 Idul Fitr 14 Basava Jayanti	
5	MAY	17	18	19	20	21	22TA	6	22 Tuesday Time Table	
6	MAY	24 T1	25T1	26T1	27	28	29DH	5		24th - 29th May AICTE - ISTE Induction / Refresher programme (FDP)
7	MAY/JUN	31	1	2	3	4	5ASD	6	5 Wednesday Tme Table	5th June IEEE KSIT SB Digital Siganal Processing Applications using MATLAB
8	JUN	7	8	9	10	11	12DH	5		11th June IETE Webinar 11th June IEEE Power of Positive Thoughts Webinar
9	JUN	14	15	16	17	18	19	6	19 Monday Time Table	14th June Internet Communication and Networking Webinar 15th June IEEE KSIT SB CREAT WIE TI Inter college Art Competation
10	JUN	21	22	23	24	25TA	26DH	5		
11	JUN/JUL	28 T2	29T2	30T2	1	2	3	6	3 Thursday time Table	2nd July IETE Webinar
12	JUL	5	6	7	8	9ASD	10DH	5		
13	JUL	12	13	14	15	16	17	6	17 Tuesday Time Table	14th July ASH in association with IEEE-WIE Webinar
14	JUL	19 T3(V,VI)	20* T3(V,VI)		22	23	24DH	4	20 *VIII Sem Last working day 21 Bakrid / Eid al Adha	19th July IEEE KSIT SB FOUS FLOW Webinar
15	JUL	26	27	28TA	29	30	31	6		29,30,31 Practice Lab
16	AUG				5 T3	6 T3	7*T3	6	7 Wednesday Tme Table	2,3,4 Practice Lab
17	AUG	9	10LT	11LT	12LT	13LT	14LT	6	14* IV &VI Last working day	10,11,12,13,14, 1st &2nd Lab Internals

Total No of Working Days : 92

Total Number of working days (Excluding holidays and Tests)=79

H	Holiday
T1, T2, T3	Tests 1,2, 3
ASD	Attendance & Sessional
DH	Declared Holiday
LT	Lab Test
TA	Test attendance

Monday	16
Tuesday	16
Wednesday	16
Thursday	16
Friday	15
Total	79

7/8/2021

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE -109

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

INDIVIDUAL TIME TABLE FOR THE YEAR - 2021 (EVEN SEMESTER)

W.E.F. : 19/4/2021

ONLINE TIME TABLE

NAME OF THE FACULTY : SUNIL KUMAR G.R. **DESIGNATION: ASSISTANT PROFESSOR**

PERIOD	1	2	11.00 AM 11.15 AM	3	4	1.15 PM 1.45 PM	5	6
TIME / DAY	9.00 AM 10.00 AM	10.00 AM 11.00 AM		11.15 AM 12.15 PM	12.15 PM 1.15 PM		1.45 PM 2.45 PM	2.45 PM 3.45 PM
MON			TEA BREAK			LUNCH BREAK	MC (18EC46) PEDAGOGY	
TUE		MC (18EC46)						
WED				MC (18EC46)				
THU	MC (18EC46)							
FRI					MC (18EC46)			

	Subject Code	Subject Name	Sem	Section	Work Load
Subject 1	18EC46	Microcontroller	IV	A	5
Lab -2	18ECL47	Microcontroller Laboratory	IV	A	4.5
Lab -1	18ECL66	Embedded Systems Laboratory	VI	A&B	1.5
Internship	17EC84	Internship/Professional Practice	VIII		2
Project	17ECP85	Project Work	VIII		2
ADDITIONAL WORK: MENTORING AND OTHERS					
TOTAL LOAD= 15 Hrs/Week					

Time Table Co-ordinator

HOD 19/4

Principal

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

IV SEMESTER TIME TABLE FOR THE YEAR 2021 (EVEN SEMESTER)

W.E.F. : 19/04/2021 **ONLINE TIME TABLE** **CLASS TEACHER : Mr. B.R.Santhosh Kumar**

SEC : 'A'

PERIOD	1	2	11.00 AM 11.15 AM	3	4	1.15 PM 1.45 PM	5	6
TIME DAY	9.00 AM 10.00 AM	10.00 AM 11.00 AM		11.15 AM 12.15 PM	12.15 PM 1.15 PM		1.45 PM 2.45 PM	2.45 PM 3.45 PM
MON	AC (18EC42)	MATHS (18MAT41)	T E A B R E A K	ES&L (18EC44)	CS (18EC43)	L U N C H B R E A K	MC (18EC46) PEDAGOGY	CS (18EC43) PEDAGOGY
TUE	CS (18EC43)	MC (18EC46)		AC (18EC42)	SS (18EC45)		ES&L (18EC44)	MATHS (18MAT41)
WED	ES&L (18EC44)	SS (18EC45)		MC (18EC46)	MATHS (18MAT41)		AC (18EC42) PEDAGOGY	SS (18EC45) PEDAGOGY
THU	MC (18EC46)	AC (18EC42)		ES&L (18EC44)	SS (18EC45)		CS (18EC43)	CPC (18CPC39/49)
FRI	AC (18EC42)	MATHS (18MAT41)		SS (18EC45)	MC (18EC46)		CS (18EC43)	ES&L(18EC44) PEDAGOGY

Sub-Code	Subject Name	Faculty Name
18MATDIP41	Additional Mathematics – II	Mrs Lakshmi C
18MAT41	Complex Analysis, Probability and□Statistical Methods	Mrs Lakshmi C
18EC42	Analog Circuits	Mr. B.R.Santhosh Kumar
18EC43	Control Systems	Mr. Praveen.A
18EC44	Engineering Statistics & Linear□Algebra	Mrs. Yeshwini V
18EC45	Signals & Systems	Mrs. Pragati. P
18EC46	Microcontroller	Mr. Sunil Kumar.G.R
18ECL47	Microcontroller Laboratory	Mr. Sunil Kumar.G.R, Mr. Praveen.A, Mr. Christo Jain S
18ECL48	Analog Circuits Laboratory	Mr. B.R.Santhosh Kumar, Mrs. Yeshwini V
18CPC39/49	Constitution of India, Professional□Ethics and Cyber Law	Mrs Anuradha V

Time Table Co-ordinator

HOD

Principal

MICROCONTROLLER

Course Code : **18EC46**	CIE Marks : 40
Lecture Hours/Week : 03	SEE Marks : 60
Total Number of Lecture Hours : 40 (8 Hours / Module)	Exam Hours:03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers.
- Familiarize the basic architecture of 8051 microcontroller.
- Program 8051 microprocessor using Assembly Level Language and C.
- Understand the interrupt system of 8051 and the use of interrupts.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051.
- Interface 8051 to external memory and I/O devices using its I/O ports.

Module-1

8051 Microcontroller: Microprocessor vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing.

L1, L2

Module -2

8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions.

L1, L2

Module-3

8051 Stack, I/O Port Interfacing and Programming: 8051 Stack, Stack and Subroutine instructions. Assembly language program examples on subroutine and involving loops.

Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status.

L1, L2, L3

Module -4

8051 Timers and Serial Port: 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin. 8051 Serial Communication- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially.

L1, L2, L3

Module -5

8051 Interrupts and Interfacing Applications: 8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt. Interfacing 8051 to ADC-0804, DAC, LCD and Stepper motor and their 8051 Assembly language interfacing programming.

L1, L2, L3

Course outcomes: At the end of the course, students will be able to:

1. Explain the difference between Microprocessors & Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and Instruction set of 8051.
2. Write 8051 Assembly level programs using 8051 instruction set.
3. Explain the Interrupt system, operation of Timers/Counters and Serial port of 8051.
4. Write 8051 Assembly language programs to generate square wave on 8051 I/O port pin using interrupt and C Programme to send & receive serial data using 8051 serial port.
5. Interface simple switches, simple LEDs, ADC 0804, LCD and Stepper Motor to 8051 using 8051 I/O ports.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "The 8051 Microcontroller and Embedded Systems – using assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth J. Ayala, 3rd Edition, Thomson/ Cengage Learning.

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

NAME OF THE FACULTY : MR. SUNIL KUMAR G. R.
COURSE CODE/NAME : 18EC46/ MICROCONTROLLER
SEMESTER/YEAR : IV 'A' / II
ACADEMIC YEAR : 2020-2021

Sl.No	Topic to be covered	Mode of Delivery	Teaching Aid	No. of Periods	Cumulative No. of Periods	Proposed Date
	MODULE 1: Introduction to Microcontroller					
1.	Introduction to Microcontroller	L+D	PPT	1	1	19-04-21
2.	Microprocessor Vs Microcontroller	L+ D	PPT	1	2	20-04-21
3.	Embedded Systems and Embedded Microcontrollers	L+ D	PPT	1	3	21-04-21
4.	8051 Architecture- Registers	L+ D	PPT	2	5	22-04-21 23-04-21
5.	Pin diagram of 8051	L+ D	PPT	1	6	24-04-21
6.	I/O ports functions	L+ D	PPT	1	7	27-04-21
7.	Internal Memory organization	L+D	PPT	2	9	28-04-21 29-04-21
8.	External Memory (ROM & RAM) interfacing	L+ D	PPT	2	11	30-04-21 3-05-21
	MODULE 2: 8051 INSTRUCTIONS SET					
9.	Addressing Modes	L+D	PPT	1	12	4-05-21
10.	Instructions classification based on addressing modes	L+D	PPT	1	13	5-05-21
11.	Data Transfer instructions	L+D	PPT	3	16	6-05-21 7-05-21 8-05-21
12.	Arithmetic instructions	L+D	PPT	2	18	10-05-21 11-05-21
13.	Logical instructions	L+D	PPT	2	20	12-05-21 17-05-21
14.	Branch instructions	L+D	PPT	2	22	18-05-21 19-05-21
15.	Bit manipulation instructions	L+D	PPT	2	24	20-05-21 21-05-21
16.	Simple Assembly language program examples (without loops) to use these	D+PS	PPT	2	26	22-05-21 26-05-21

	instructions					
MODULE 3: 8051 STACK, I/O PORT INTERFACING AND PROGRAMMING						
17.	8051 Stack	L+D	PPT	1	27	28-05-21
18.	Stack and Subroutine instructions	L+D	PPT	1	28	31-05-21
19.	Assembly language program examples on subroutine	D+PS	PPT	2	30	01-06-21 02-06-21
20.	Subroutine involving loops - Delay subroutine	L+D	PPT	2	32	03-06-21 04-06-21
21.	Interfacing simple switch and LED to I/O ports with respect to switch status	D+PS	PPT	2	34	05-06-21 07-06-21
MODULE 4: 8051 TIMERS AND SERIAL PORT						
22.	8051 Timers and Counters – Operation	L+D	PPT	1	35	08-06-21
23.	Assembly language programming to generate a pulse using Mode-1	D+PS	PPT	1	36	09-06-21
24.	Assembly language programming to generate a square wave using Mode-2 on a port pin	D+PS	PPT	1	37	10-06-21
25.	8051 Serial Communication- Basics of Serial Data Communication	L+D	PPT	1	38	11-06-21
26.	RS-232 standard	L+D	PPT	1	39	14-06-21
27.	9 pin RS232 signals	L+D	PPT	1	40	15-06-21
28.	Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially	D+PS	PPT	3	43	16-06-21 17-06-21 18-06-21
MODULE 5: 8051 INTERRUPTS AND INTERFACING APPLICATIONS						
29.	8051 Interrupts	L+D	PPT	1	44	19-06-21
30.	8051 Assembly language programming to generate an external interrupt using a switch	D+PS	PPT	2	46	21-06-21 22-06-21
31.	8051 C programming to generate a square waveform on a port pin using a Timer interrupt	D+PS	PPT	1	47	23-06-21
32.	Interfacing 8051 to ADC-0804	L+D	PPT	1	48	24-06-21
33.	Interfacing DAC	L+D	PPT	1	49	25-06-21
34.	Interfacing 8051 to LCD and Stepper motor	L+D	PPT	1	50	1-07-21
35.	Interfacing Stepper motor	L+D	PPT	1	51	2-07-21
36.	Assembly language interfacing programming	D+PS	PPT	3	54	3-07-21 5-07-21 6-07-21

Text Books:

1. The 8051 Microcontroller and Embedded Systems – using assembly and C ", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006.

2. The 8051 Microcontroller", Kenneth J. Ayala, 3rd Edition, Thomson/Cengage Learning

Reference Books:

1.The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.

2. Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005

WEB MATERIALS:

W1: https://nptel.ac.in/courses/117104072/
W2: https://freevideolectures.com/course/3018/microprocessors-and-microcontrollers/22
W3: https://www.edgefxkits.com/blog/application-of-microcontroller-in-technology/
W4: http://www.circuitstoday.com/8051-microcontroller
W5: https://www.electronicshub.org/8051-microcontroller
W6: https://www.youtube.com/watch?v=FL9FhznJw2E&t=199s
W7: https://www.youtube.com/watch?v=EOAXox9XzTI&t=180s
W8: https://www.youtube.com/watch?v=pjcp7qLPPFw&t=1s
W9: https://www.youtube.com/watch?v=6ai2wl8-jv4&t=488s
W10: https://www.youtube.com/watch?v=pihAdSek7oM

Details for the teaching Aids

1. Power Point Presentation
2. Microsoft Teams, Keil Software

Course In charge **Module Coordinator** **HOD**

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

Department of Electronics and Communication

Assignment – I

Course Title : MICROCONTROLLER
Course Code : 18EC46

Date: 17-05-2021
Marks: 10

Note:

- **Write the Answers for the following questions and submit it before 22-05-2021**
- **Scan and save as PDF/image and send it to sunilkumargr@ksit.edu.in**
- **Save the document with USN only with e-mail subject as Assignment-I**

Q No.	Question	Marks	CO Mapping	K-Level
1	With neat diagrams explain the architecture of 8051 microcontroller, internal memory and PSW.	2	CO1	K3 Applying
2	Differentiate between Microprocessor and Microcontroller.	2	CO1	K3 Applying
3	With a neat diagram explain the pin details of 8051 microcontroller.	2	CO1	K3 Applying
4	Explain assembler directives and addressing modes of 8051 microcontroller.	2	CO2	K3 Applying
5	Explain the following instructions with an example for each: i) MOVC A, @A+DPTR, ii) POP direct, iii) XCHD A, @Ri, iv) DIV AB, v) CPL A	2	CO2	K3 Applying

Course In-charge

Module Coordinator

HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

Department of Electronics and Communication

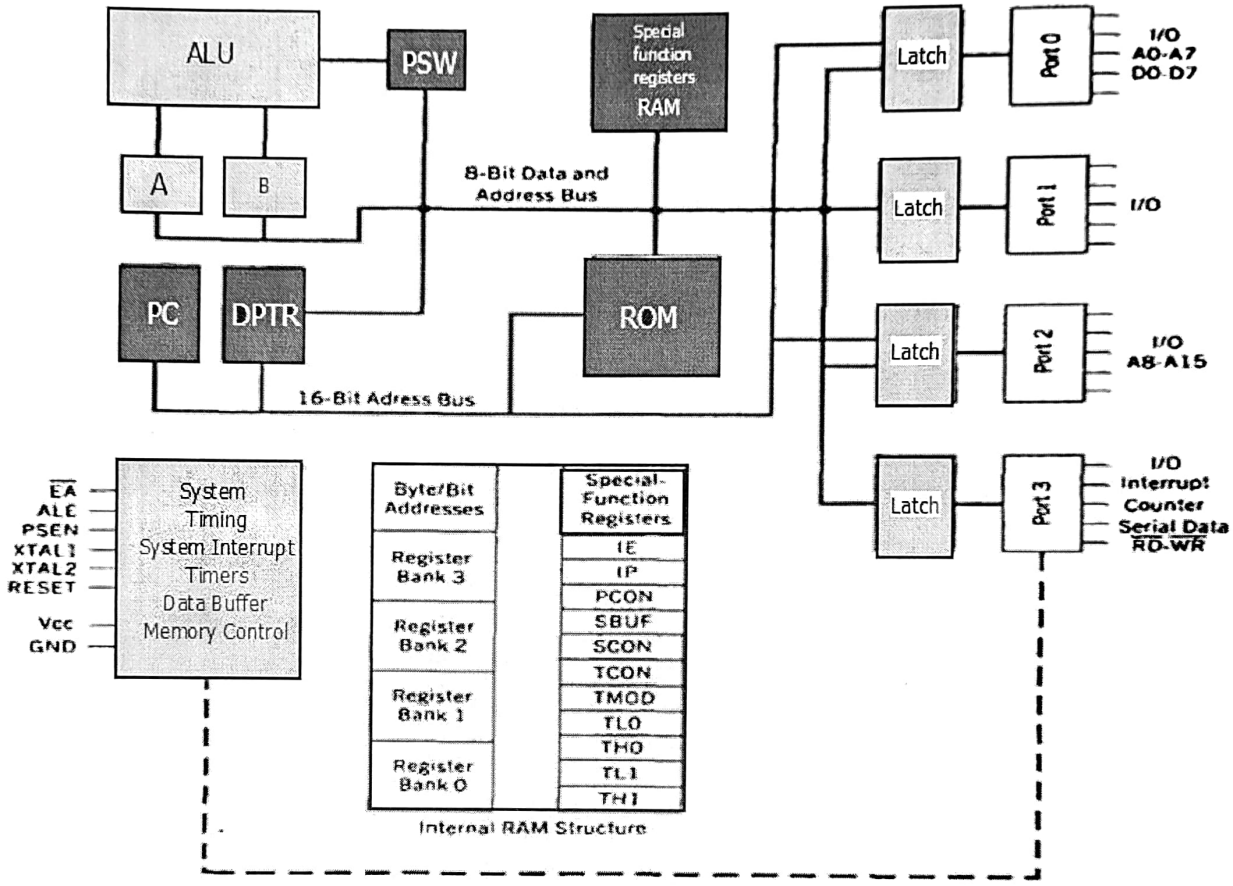
Assignment –1 Question and Scheme

Course Title :MICROCONTROLLER
Course Code: 18EC46 (AY-2020-21)

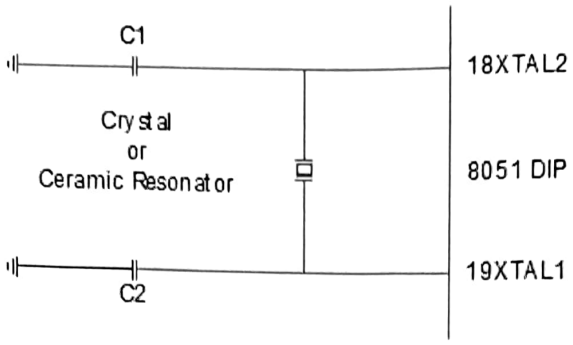
Date:17-05-2021
Marks: 10

Note: Write the Answers for the following questions and submit it before 22-05-2021

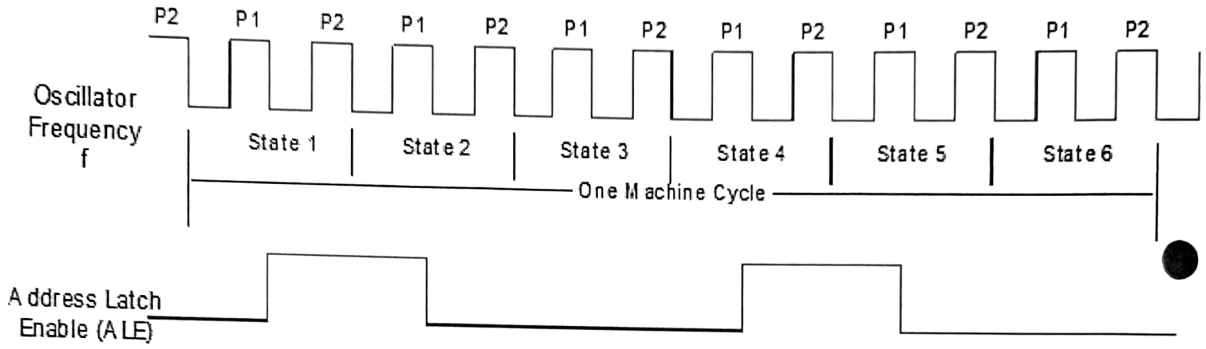
1. **With neat diagrams explain the architecture of 8051 microcontroller, internal memory and PSW.**



- 8051 is an 8-bit microcontroller, The ALU performs one 8-bit operation at a time
- 8-bit data bus
- 16-bit address bus, The 16 bit address bus can address a 64K(2^{16}) byte code memory space and a separate 64K byte of data memory space
- 8051 has 4K on-chip read only code memory (ROM)
- 128 bytes of internal Random Access Memory (RAM)
- There are 34, 8-bit general purpose registers
- There are 21 SFRs.
- Two 16-bit timers/ counter
- Four 8-bit I/O ports (3 of them are dual purpose). One of them used for serial port
- 5+1 Interrupts are there: 2 timer interrupts, 2 external hardware interrupts and one serial interrupt
- 8051 is a 40 pin IC



Crystal or Ceramic Resonator Oscillator Circuit



CY	AC	F0	RS1	RS0	OV	–	P

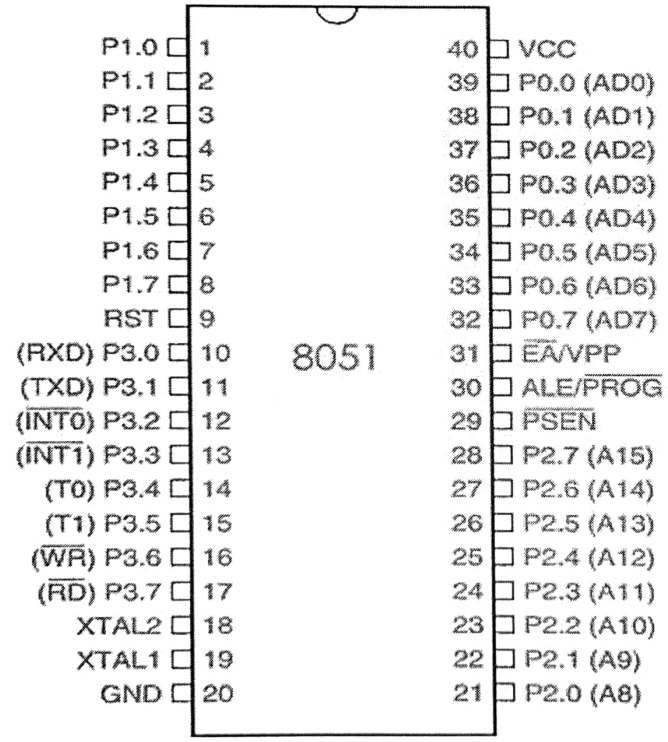
CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1.
RS0	PSW.3	Register Bank selector bit 0.
OV	PSW.2	Overflow flag.
–	PSW.1	User-definable bit.
P	PSW.0	Parity flag. Set/cleared by hardware each instuction cycle to indicate an odd/even number of 1 bits in the accumulator.

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

2. **Differentiate between Microprocessor and Microcontroller.**

Sl. No.	MICROPROCESSOR	MICROCONTROLLER
1	MP have many operational codes for moving data from external memory to the CPU	MC may have one or two
2	MP may have one or two bit handling instructions	MC will have many
3	Less multifunction pins on IC	Many multifunction pins on IC
4	MP takes many instructions to read and write data from external memory	MC takes few instructions to read and write da from external memory
5	Generally higher core clock frequency	Generally lower core clock frequency
6	High performance pipelined CPU Architecture	Low performance pipelined CPU Architecture
7	General purpose processor	Application specific single chip solution

3. **With a neat diagram explain the pin details of 8051 microcontroller.**

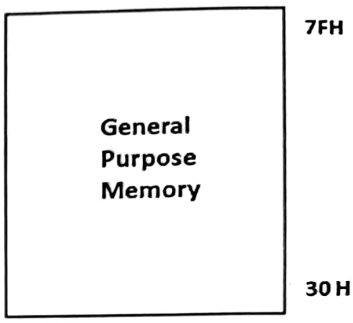


40 - PIN DIP

R7	1FH	
R6	1EH	
R5	1DH	
R4	1CH	
R3	1BH	Bank 3
R2	1AH	
R1	19H	
R0	18H	
R7	17H	
R6	16H	
R5	15H	
R4	14H	
R3	13H	Bank 2
R2	12H	
R1	11H	
R0	10H	
R7	0FH	
R6	0EH	
R5	0DH	
R4	0CH	
R3	0BH	Bank1
R2	0AH	
R1	09H	
R0	08H	
R7	07H	
R6	06H	
R5	05H	
R4	04H	
R3	03H	
R2	02H	Bank0
R1	01H	
R0	00H	

7F							78	2F
77							70	2E
6F							68	2D
67							60	2C
5F							58	2B
57							50	2A
4F							48	29
47							40	28
3F							38	27
37							30	26
2F							28	25
27							20	24
1F							18	23
17							10	22
0F							08	21
07	06	05	04	03	02	01	00	20

Bit/Byte addressable memory area



Byte address	Bit address								
FF									
F0	F7	F6	F5	F4	F3	F2	F1	F0	B
E0	E7	E6	E5	E4	E3	E2	E1	E0	ACC
D0	D7	D6	D5	D4	D3	D2	D1	D0	PSW
B8	--	--	--	BC	BB	BA	B9	B8	IP
B0	B7	B6	B5	B4	B3	B2	B1	B0	P3
A8	AF	--	--	AC	AB	AA	A9	A8	IE
A0	A7	A6	A5	A4	A3	A2	A1	A0	P2
99	not bit-addressable								SBUF
98	9F	9E	9D	9C	9B	9A	99	98	SCON
90	97	96	95	94	93	92	91	90	P1
8D	not bit-addressable								TH1
8C	not bit-addressable								TH0
8B	not bit-addressable								TL1
8A	not bit-addressable								TL0
89	not bit-addressable								TMOD
88	8F	8E	8D	8C	8B	8A	89	88	TCON
87	not bit-addressable								PCON
83	not bit-addressable								DPH
82	not bit-addressable								DPL
81	not bit-addressable								SP
80	87	86	85	84	83	82	81	80	P0

Special Function Registers

Figure 5-2. SFR RAM Address (Byte and Bit)

4. Explain assembler directives and addressing modes of 8051 microcontroller.

There are 5 addressing modes:

Immediate:

- The source operand is a constant
- The data is immediately available next to destination
- Immediate data must be prefixed by the '#' sign

Ex: MOV A,#25H – 0010 0101

Register:

- It involves the use of registers to hold the data to be manipulated

Ex: MOV A,R0

Direct:

- In this mode, the data is in a RAM memory location, whose address is known, and this address is given as a part of the instruction

Ex: MOV R0,40H

Register Indirect:

- In this mode, a register is used as a pointer to the data
- If the data is inside the CPU, only register R0 and R1 are used for this purpose
- In other words R2 to R7 cannot be used to hold the address of an operand located in RAM when using this addressing mode
- When R0 and R1 hold the address of RAM locations, they must be prefixed by '@' sign

Ex: MOV A,@R0

Indexed:

- It is widely used in accessing data elements of look-up table entries located in the program ROM space of the 8051
- The instruction used for this purpose is MOVC A, @A+DPTR
- A+DPTR collectively form the address of the data element stored in on-chip ROM
- Because the data elements are stored in the Program (Code) space ROM of the 8051, the instruction MOVC is used instead of MOV. The C mean Code.

5. Explain the following instructions with an example for each: i) MOVC A, @A+DPTR, ii) POP direct, iii) XCHD A, @Ri, iv) DIV AB, v) CPL A

MOVC A,@A+DPTR	1	2 (24)	Indexed	Copy 8-bit data from code memory pointed by sum of A & DPTR registers to accumulator
POP direct	2	2 (24)	Direct	Copy top of stack contents to direct memory location and then decrement stack pointer
XCHD A, @Ri	1	1(12)	indirect	Exchange the lower order bits of accumulator with RAM memory location contents pointed by register
DIV AB	1	4(48)	Register	Divide acc by B and store quotient in acc & reminder in B register
CPL A	1	1(12)	Register	Logically XOR immediate value and ACC contents and store the result in ACC

Course In-charge Module Coordinator HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

Department of Electronics and Communication

Assignment – II

Course Title : MICROCONTROLLER
Course Code :18EC46

Date: 19-06-2021
Marks: 10

Note: Answer ANY FIVE of the following questions and submit it before 26-06-2021
Scan and save as PDF/image and send it to sunilkumargr@ksit.edu.in
Save the document with USN only, with e-mail subject as Assignment-II

Q No.	Question	Marks	CO Mapping	K-Level
1.	Write an ALP to transfer data blocks from external source memory location to external destination memory location.	2	CO2	K3 Applying
2.	Write an ALP to transfer data blocks from internal source memory location to external destination memory location.	2	CO2	K3 Applying
3.	Write an ALP to exchange data blocks from external source memory location to external destination memory location.	2	CO2	K3 Applying
4.	Write an ALP to exchange data blocks from internal source memory location to external destination memory location.	2	CO2	K3 Applying
5.	Write an ALP to generate Fibonacci series.	2	CO3	K3 Applying
6.	Write an ALP to find LCM of two 8-bit numbers.	2	CO3	K3 Applying
7.	Write an ALP to find GCD of two 8-bit numbers.	2	CO3	K3 Applying
8.	Write an ALP to check whether the given number is prime or not?	2	CO3	K3 Applying
9.	Write an ALP to check whether the given 8-bit number is a Bit-wise Palindrome or not	2	CO3	K3 Applying
10.	Write an ALP to check whether the given word is a Palindrome or not?	2	CO3	K3 Applying
11.	Write a code to push R0, R1 and R2 of bank-0 onto the stack memory and pop them into R5, R6 and R7 of bank-3.	2	CO3	K3 Applying
12.	Write a program to store FFH into RAM locations from 50H to 6FH .	2	CO3	K3 Applying
13.	Write a program to find y where $y = x^2 + 2x + 5$, assume x between 0 to 9.	2	CO3	K3 Applying
14.	Write a program to find whether the given number is a '2 out of 5' code or not?	2	CO3	K3 Applying
15.	Write a program to see whether the given number is divisible by 8 or not?	2	CO4	K3 Applying
16.	Write a program to find the number of zero's in register R2.	2	CO4	K3 Applying
17.	Write a program to find the number of positive and negative numbers in an array.	2	CO4	K3 Applying
18.	Write a program to complement content of accumulator 62500 times.	2	CO4	K3 Applying

Course In-charge

Module Coordinator

HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

Department of Electronics and Communication

Assignment – II Question and Scheme

Course Title : MICROCONTROLLER
Course Code :18EC46 (AY-2020-21)

Date : 19-06-2021
Marks : 10

Note: Write the Answers for the following questions and submit it before 26-06-2021

1. Write an ALP to transfer data blocks from external source memory location to external destination memory location.

```
ORG 0000H
            MOV DPTR,#8000H
            MOV R0, #00H
            MOV R1, #50H
            MOV R2,#05H
REPEAT:     MOV DPL, R0
            MOV A,@DPTR
            MOV DPL, R1
            MOV @DPTR,A
            INC R0
            INC R1
            DJNZ R2,REPEAT
HERE:       SJMP HERE
END
```

2. Write an ALP to exchange data blocks from internal source memory location to external destination memory location.

```
ORG 0000H
            MOV R0,#10H
            MOV DPTR, #8000H
            MOV R2,#05H
REPEAT:     MOV A,@R0
            XCH A,@DPTR
            MOV @R0,A
            INC R0
            INC DPTR
            DJNZ R2,REPEAT
HERE:       SJMP HERE
END
```

3. Write a code to push R0, R1 and R2 of bank-0 onto the stack memory and pop them into R5, R6 and R7 of bank-3.

```
ORG 0000H
            PUSH 00H
            PUSH 01H
            PUSH 02H
            SETB PSW.3
            SETB PSW.4
            POP 05H
            POP 06H
            POP 07H
END
```

4. Write a program to store FFH into RAM locations from 50H to 6FH.

```
ORG 0000H
        MOV R0,#50H
        MOV R2, #16
REPEAT: MOV @R0, #0FFH
        INC R0
        DJNZ R2, REPEAT
END
```

5. Write a program to find y where $y = x^2 + 2x + 5$, assume x between 0 to 9.

```
ORG 0000H
        MOV R0,#50H
        MOV A, @R0
        MOV A, B
        MUL AB
        MOV R2, A
        MOV A, @R0
        MOV B, #02H
        MUL AB
        ADD A, #05H
        ADD A, R2
END
```

Course In-charge Module Coordinator HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

Department of Electronics and Communication

Assignment – III

Course Title : MICROCONTROLLER
Course Code : 18EC46

Date: 01-08-2021
Marks: 10

Note:

- **Write the Answers for the following questions and submit it before 04-08-2021**
- **Scan and save as PDF/image and send it to sunilkumargr@ksit.edu.in**
- **Save the document with USN only with e-mail subject as Assignment-III**

Q No.	Question	Marks	CO Mapping	K-Level
1.	Write an ALP to interface simple switch and LED to I/O ports to switch on/off LED with respect to switch status.	2	CO4	K3 Applying
2.	Assume XTAL = 11.0592 MHz, write a program to generate a square wave of 2 kHz frequency on pin P1.5.	2	CO4	K3 Applying
3.	List out the steps to program the 8051 to transfer data serially.	2	CO5	K3 Applying
4.	Explain the interrupt vector table and IE register.	2	CO5	K3 Applying
5.	With a neat interfacing diagram, write an ALP to program 8051 to rotate a stepper motor in clockwise and anticlockwise directions.	2	CO5	K3 Applying

Course In-charge

Module Coordinator

HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

Department of Electronics and Communication

Assignment – III Question and Scheme

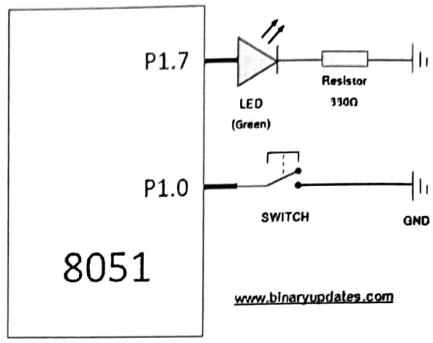
Course Title : MICROCONTROLLER
Course Code :18EC46 (AY-2020-21)

Date : 01-08-2021
Marks : 10

Note: Write the Answers for the following questions and submit it before 04-08-2021

1. Write an ALP to interface simple switch and LED to I/O ports to switch on/off LED with respect to switch status.

```
ORG 0000H
        SETB P1.0
REPEAT:MOV C,P1.0
        MOV P1.7,C
        SJMP REPEAT
END
```



2. Assume XTAL = 11.0592 MHz, write a program to generate a square wave of 2 kHz frequency on pin P1.5.

Given, fc = 11.0592 MHz
Time Period, t= 1/11.0592 MHz = 0.0904 µsec
Machine Cycle Period, T = 0.0904 µsec x 12 = 1.085 µsec
To find initial values TH and TL:
Fc=2KHz, Total Time, T= 1/2KHz = 500 µsec, T/2=250µsec
1. 250 µsec /1.085 µsec = 230.414 = 230
2. 65536 – 230 = 65306
3. FF1A
4. TH = FF, & TL = 1A

```
ORG 0000H
        MOV TMOD, #01H
RE:     MOV TL0, #1AH
        MOV TH0, #0FFH
        SETB TR0
ST:     JNB TF0, ST
        CPL P1.5
        CLR TR0
        CLR TF0
        SJMP RE
END
```

3. List out the steps to program the 8051 to transfer data serially.

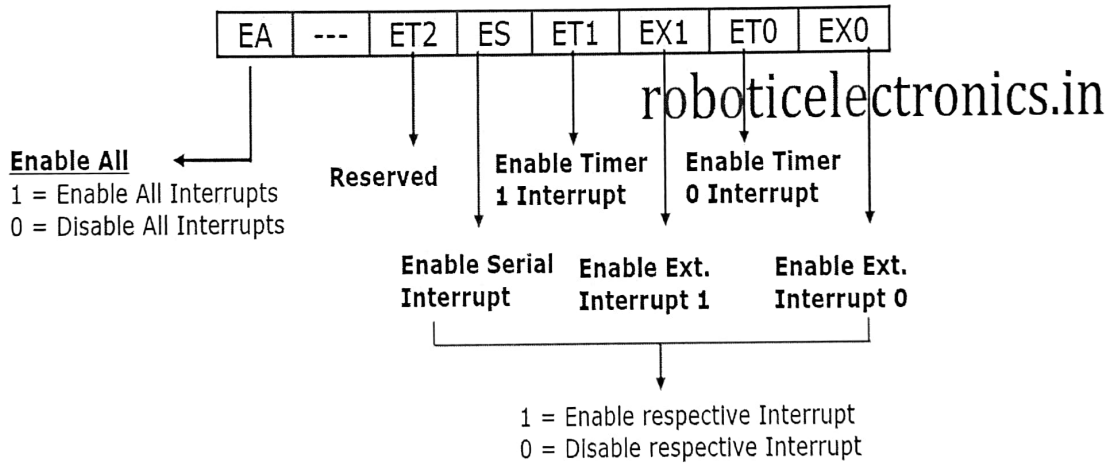
1. TMOD register is loaded with the value 20H, indicating the use of Timer 1 in mode 2 (8-bit auto-reload) to set the baud rate
2. The TH1 is loaded with one of the values like FDH, F4H, E8H etc.. to set the baud rate for serial data transfer

3. The SCON register is loaded with the value 50H, indicating serial mode 1, where an 8-bit data is framed with start and stop bits
4. TR1 is set to 1 to start Timer 1
5. TI is cleared by the "CLR TI" instruction
6. The character byte to be transferred serially is written into the SBUF register
7. The TI flag bit is monitored with the use of the instruction "JNB TI, xx" to see if the character has been transferred completely
8. To transfer the next character, go to step 5

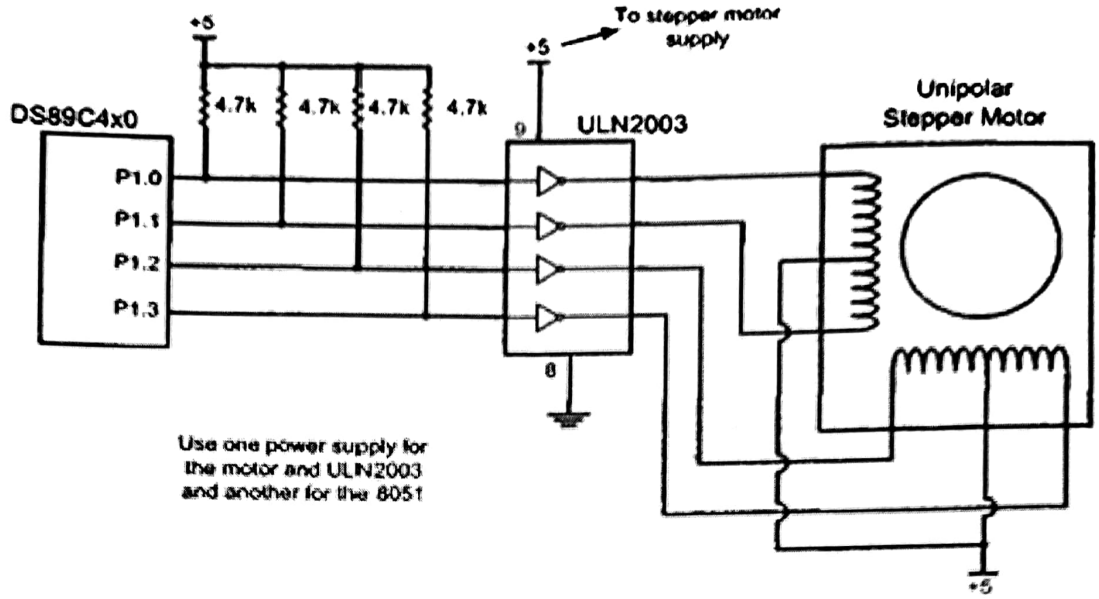
4. Explain the interrupt vector table and IE register.

Interrupt	ROM Location (Hex)	Pin	Flag Clearing
Reset	0000	9	Auto
External hardware interrupt 0 (INT0)	0003	P3.2 (12)	Auto
Timer 0 interrupt (TF0)	000B		Auto
External hardware interrupt 1 (INT1)	0013	P3.3 (13)	Auto
Timer 1 interrupt (TF1)	001B		Auto
Serial COM interrupt (RI and TI)	0023		Programmer clears it.

IE - Interrupt Enable (SFR) [Bit-Addressable As IE.7 to IE.0]



5. With a neat interfacing diagram, write an ALP to program 8051 to rotate a stepper motor in clockwise and anticlockwise directions.




```
org 0000h
        mov p1,#0ffh
        mov a,#77h
        mov p2,a
turn: jnb p1.0,cw
rr a
acall delay
        mov p2,a
sjmp turn
cw:   rl a
acall delay
        mov p2,a
sjmp turn

delay: mov R2,#255
h1:     mov R3,#255
h2:     djnz R3,h2
djnz R2,h1
         ret
end
```

Course In-charge

Module Coordinator

HOD-ECE

K.S.INSTITUTEOFTECHNOLOGY,BANGALORE-560109
I SESSIONAL TEST QUESTION PAPER 2020–21 EVEN SEMESTER

USN | | | | | | | | | | |

SetA

Degree : BE
Branch : Electronics & Communication Engg
SubjectTitle : MICROCONTROLLER
Duration : 90Minutes

Semester : IVA&B
Subject Code : 18EC46
Date : 26.05.2021
Max Marks : 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	CO mapping	K-Level
	PART-A			
1(a)	With neat block diagram explain features of microcontroller 8051.	6	CO1	K3 Applying
(b)	Write a short not criteria for choosing a microcontroller.	6	CO1	K3 Applying
(c)	Write an interfacing diagram 8051 microcontroller interfaced to 8k bytes of ROM and 8k bytes of RAM.	6	CO1	K3 Applying
	OR			
2(a)	With neat diagram explain the internal memory structure of 8051 microcontroller.	6	CO1	K3 Applying
(b)	Bring out the difference between Microprocessor and Microcontroller.	6	CO1	K3 Applying
(c)	Explain the following pins with respect memory interfacing: ALE, EA! and PSEN!	6	CO1	K3 Applying
	PART-B			
3(a)	Explain 5 different addressing modes with examples.	6	CO2	K3 Applying
(b)	Explain the following instructions, also mention how many bytes it takes to store in ROM: i) PUSH 40h, ii) XCHD A, @R0, iii) DIV AB, iv) SWAP A, v) CPL A, vi) DAA	6	CO2	K3 Applying
	OR			
4(a)	Define assembler directives. With example explain all the assembler directives supported by 8051 microcontroller.	6	CO2	K3 Applying
(b)	Show the status of CY, AC and P flags after the execution of following instructions: MOV A, #9CH, ADD A, #64H	6	CO2	K3 Applying

Course In-Charge

Module Coordinator

HOD-ECE

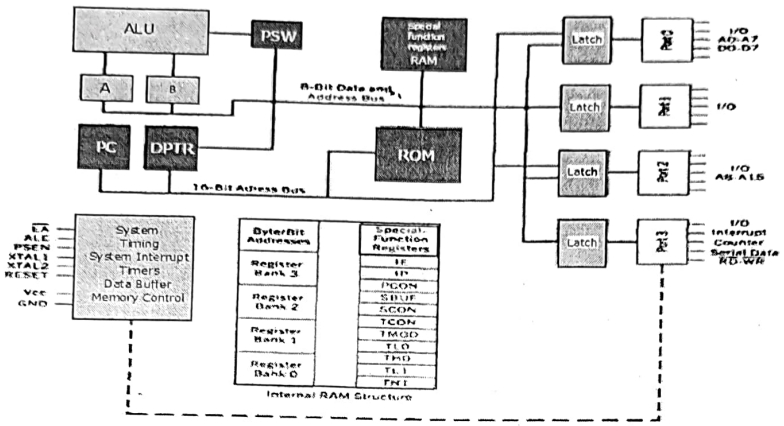
K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

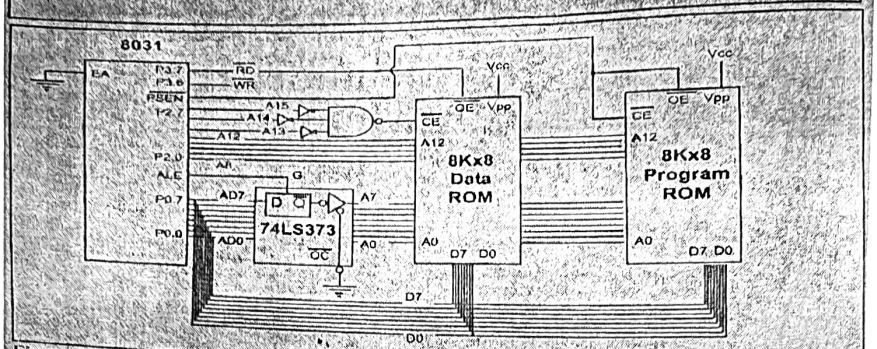
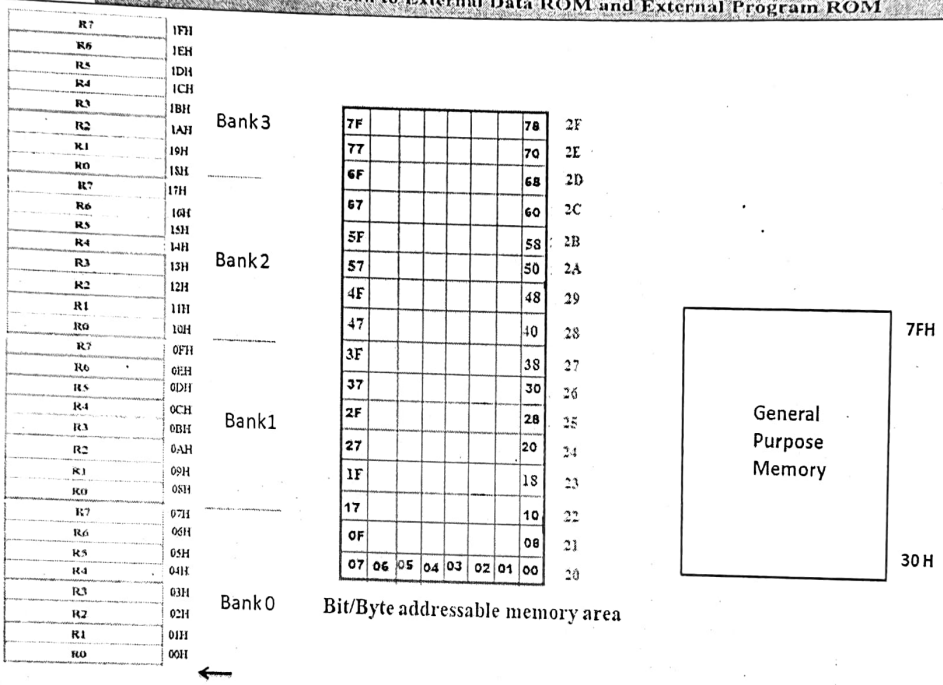
I SESSIONAL TEST scheme 2020 – 21 EVEN SEMESTER

SET – A

Degree	: BE	Semester :	IV A & B
Branch	: Electronics and Communication Engg	Course Code :	18EC46
Course Title	: Microcontroller	Date :	26/05/21
Duration	: 90 Minutes	Max Marks :	30

Note: Answer ONE full question from each part.

Q No.	Question	Marks
1 (a)		6
	➢ 8051 is an 8-bit microcontroller, The ALU performs one 8-bit operation at a time ➢ 8-bit data bus ➢ 16-bit address bus, The 16 bit address bus can address a 64K(2^{16}) byte code memory space and a separate 64K byte of data memory space ➢ 8051 has 4K on-chip read only code memory (ROM) ➢ 128 bytes of internal Random Access Memory (RAM) ➢ There are 34, 8-bit general purpose registers ➢ There are 21 SFRs. ➢ Two 16-bit timers/ counter ➢ Four 8-bit I/O ports (3 of them are dual purpose). One of them used for serial port ➢ 5+1 Interrupts are there: 2 timer interrupts, 2 external hardware interrupts and one serial interrupt ➢ 8051 is a 40 pin IC	
(b)	1. MC must meet the task at hand efficiently and cost effectively a. Speed. Highest Speed? b. Packaging. DIP or QFP ->space, assembling, and prototyping the end product c. Power Consumption. Critical for battery-powered products d. The amount of RAM and ROM on chip e. The number of I/O pins and the timer on the chip f. How easy it is to upgrade to higher performance or lower power consumption versions g. Cost per unit 2. How easy it is to develop products around it. The availability of an assembler, debugger, compiler, emulator, technical support. 3. Ready availability in needed quantities both now and in the future is more important than first two criteria.	6

(c)	**Example 14-11** Show the design of an 8031-based system with 8K bytes of program ROM and 8K bytes of data ROM. **Solution:** Figure 14-14 shows the design. Notice the role of PSEN and RD in each ROM. For program ROM, PSEN is used to activate both OE and CE. For data ROM, we use RD to activate OE, while CE is activated by a simple decoder.  Figure 14-14. 8031 Connection to External Data ROM and External Program ROM	6
2 (a)	 Explanation on Bank resgister, Bit addressable area, Stack memory amd scratch pad and SFRs	6
(b)		6

Sl. No.	MICROPROCESSOR	MICROCONTROLLER
1	MP have many operational codes for moving data from external memory to the CPU	MC may have one or two
2	MP may have one or two bit handling instructions	MC will have many
3	Less multifunction pins on IC	Many multifunction pins on IC
4	MP takes many instructions to read and write data from external memory	MC takes few instructions to read and write data from external memory

	5	Generally higher core clock frequency	Generally lower core clock frequency	
	6	High performance pipelined CPU Architecture	Low performance pipelined CPU Architecture	
	7	General purpose processor	Application specific single chip solution	

(C)

1. External Access (EA!) Pin: is an input pin and is connected to either Vcc or GND, it cannot be left unconnected.
   - when connected to Vcc the program code is stored in the Microcontroller on-chip ROM.
   - when connected to GND, the program code is stored in external ROM.
2. ALE: is an output pin, when ALE=1, P0 is used for the address path and when ALE=0, P0 is used to send/receive data
   - To extract the address from the P0 pin, we connect P0 to a 74LS373 latch IC, and use ALE pin to latch the address as shown in fig below:
   - The extracting of address from P0 is called address/data demultiplexing
3. Program Store Enable (PSEN!): is an output pin connected to the OE! Pin of a ROM
   - To access external ROM containing program code, the 8051 uses the PSEN! Signal
   - When EA! Pin connected to GND, the 8051 fetches opcodes from external ROM by using PSEN!,
   - When EA! Pin is connected to Vcc, the 8051 do not activate the PSEN! Pin – this indicates that the on-chip ROM contains program code

6

3(a)

There are 5 addressing modes: i) immediate, ii) register, iii) direct, iv) register indirect and v) indexed: Examples: i) MOV A, #25H, ii) MOV A, R0, iii) MOV R0, 40H, iv) MOV A, @R0, v) MOVC A, @A+DPTR

6

(b)

PUSH direct	2	2 (24)	Direct	Increment stack pointer register by one and then store the contents of direct memory location
XCHD A, @Ri	1	1(12)	indirect	Exchange the lower order bits of accumulator with RAM memory location contents pointed by register
DIV AB	1	4(48)	Register	Divide acc by B and store quotient in acc & reminder in B register
SWAP A	1	1 (12)	Register	Swap nibbles within the Accumulator
CPL A	1	1 (12)	Register	Complement the contents of Accumulator
DA A	1	1 (12)	Register	Decimal Adjust Accumulator after addition

6

4(a)

The more widely used directives of the 8051 are: ORG, EQU and END

ORG (origin):

- The ORG directive is used to indicate the beginning of the address
- The number that comes after ORG can be either in hex or in decimal
- If the number is not followed by H, it is decimal and the assembler will convert it to hex
- Some assembler use ".ORG" instead "ORG" for the origin directive

EQU (equate):

- This is used to define a constant without occupying a memory location
- The EQU directive does not set aside storage for a data item but associates a constant

6

	value with a data label so that when the label appears in the program, its constant value will be substituted for the label Ex: COUNT EQU 25 .... MOV R3,#COUNT END Directive: ➢ Another important pseudocode is the END directive ➢ This indicates to the assembler the end of the source (asm) file ➢ The END directive is the last line of an 8051 program, meaning that in the source code anything after the END directive is ignored by the assembler ➢ Some assemblers use ".END" instead of "END"	
(b)	9C+64 = 100 With CY=1, AC=1 and P=0	**6**

Course In-charge

Module Coordinator

HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
II SESSIONAL TEST QUESTION PAPER 2020 – 21 EVEN SEMESTER

SET – A

USN										

Degree : BE
Branch : Electronics and Communication Engg
Course Title : Microcontroller
Duration : 90 Minutes

Semester : IV A & B
Course Code : 18EC46
Date : 30/06/21
Max Marks : 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	CO mapping	K-Level
	PART-A			
1(a)	**Write** a program to find y where $y = x^2 + 2x + 5$, assume x between 0 to 9.	6	CO3	K3 Applying
(b)	Assume that register 'A' is loaded with number 'N' (any integer value from 0 to 255). **Write** a program to count the number of ones in even numbered bits of accumulator.	6	CO3	K3 Applying
(C)	With the help of neat interfacing diagram, **construct** an ALP to monitor P1.5 bit. When it is high turn on odd LEDs connected to P2. If it is low turn on even LEDs connected to P3.	6	CO3	K3 Applying
	OR			
2(a)	**Write** a program to copy the value 55H into RAM locations 40H to 45H using 1) Direct addressing, without using loop. 2) Register indirect addressing without using loop.	6	CO3	K3 Applying
(b)	**Write** a code to push R0, R1 and R2 of bank-0 onto the stack memory and pop them into R5, R6 and R7 of bank-3. With a neat diagram show the changes before and after execution.	6	CO3	K3 Applying
(C)	With the help of neat interfacing diagram, **construct** an ALP to read 8 switches connected to port-1 and display switch positions on port-2 through LEDs connected to port-2.	6	CO3	K3 Applying
	PART-B			
3(a)	**Explain** the following instructions: 1) JBC bit, rel, 2) RET, 3) CJNE A, #data, rel, 4) DJNZ direct, rel, 5) NOP, 6) ORL C, /bit.	6	CO2	K3 Applying
(b)	**Describe** the various modes of operation of 8051 Timers	6	CO4	K3 Applying
	OR			
4(a)	**Discuss** the three address ranges that are utilized by jump and call instructions.	6	CO2	K3 Applying
(b)	With neat diagrams **explain** the following registers of Timer/Counter: THx, TLx, TMOD, TCON	6	CO4	K3 Applying

Course In-charge

Module Coordinator

HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

II SESSIONAL TEST Scheme 2020 – 21 EVEN SEMESTER

SET – A

Degree	: **BE**	**Semester :**	**IV A & B**
Branch	: **Electronics and Communication Engg**	**Course Code :**	**18EC46**
Course Title	: **Microcontroller**	**Date :**	**30/06/21**
Duration	: **90 Minutes**	**Max Marks :**	**30**

Note: Answer ONE full question from each part.

Q No.	Question	Marks

1 (a)	ORG 0000H
	MOV R0,#10H
	MOV A,@R0
	MOV B,A
	MUL AB
	MOV B,A
	MOV A,@R0
	ADD A,@R0
	ADD A,B
	ADD A,#05H
	INC R0
	MOV @R0,A
	END
		6

(b)	ORG 0000H
	MOV R0, #04H
	REPEAT: RRC A
	JNC SKIP
	INC R1
	SKIP: RRC A
	DJNZ R0, REPEAT
	MOV 10H, R1
	END
		6

(C)	ORG 0000H SETB P1.5 AGAIN: JNB P1.5, EVEN MOV P2, #0AAH JMP SKIP EVEN: MOV P3, #55H SKIP: SJMP AGAIN END	6

2 (a)	ORG 0000H
	MOV A, #55H
	MOV 40H, A
	MOV 41H, A
	MOV 42H, A
	MOV 43H, A
	MOV 44H, A
	MOV 45H, A
	END
	
	ORG 0000H
	MOV A, #55H
	MOV R0, #40H
	MOV @R0, A
	INC R0
	MOV @R0, A
	INC R0
	MOV @R0, A
	INC R0
	MOV @R0, A
	INC R0
	MOV @R0, A
	INC R0
	MOV @R0, A
		6

END

(b)

```
ORG 0000H
PUSH R0
PUSH R1
PUSH R2
SETB PSW.3
SETB PSW.4
POP R5
POP R6
POP R7
END
```

6

(C)

```
ORG 0000H
        MOV P1, #0FFH
REPEAT: MOV A, P1
        MOV P2, A
        SJMP REPEAT
END
```

6

3 (a)

JBC bit, rel	3	2(24)	Bit	If bit address value=1 make a jump to relative address and then make bit address value=0
RET	3	2(24)		Return from Subroutine
CJNE A, #data, rel	3	2(24)	Immediate	Compare immediate value to ACC and jump if not equal
DJNZ direct, rel	3	2(24)	Direct	Decrement direct byte and jump if not zero
NOP	1	1(12)		No operation
ORL C, /bit	2	2(24)	/Direct	Logically OR the complement of memory bit with Carry flag bit and store the result in carry flag

6

(b)

Mode	M1	M0	Operation Mode
0	0	0	13-bit timer mode 8-bit T/C THx with TLx as 5-bit prescalar
1	0	1	16-bit timer mode 16-bit T/C THx and TLx are cascaded; there is no prescaler
2	1	0	8-bit auto reload T/C THx holds a value that is to be reloaded into TLx each time it overflows
3	1	1	Split timer mode

6

4 (a)

LJMP (long jump) and SJMP (short jump):

- LJMP is a 3-byte instruction in which the first byte is the opcode, and the second and third bytes represent the 16-bit address of the target location from 0000 to FFFFh
- SJMP is a 2-byte instruction, the first byte is the opcode and the second byte is the relative address of the target location
- The relative address range of 00 to FFh is divided into forward and backward jumps; i.e., within

6

-128 to +127 bytes of memory relative to the address of the current PC

- If the jump is forward, the target address can be within a space of 127 bytes from the current PC
- If the target address is backward, the target address can be within -128 bytes from the current PC
- Deciding which one to use depends on the target address
- LCALL is a three byte instruction, the first byte is the opcode and the second and third bytes are used for the address of the target subroutine
- LCALL can be used to call subroutines located anywhere within the 64K-byte address space of the 8051
- ACALL is a two byte instruction, the target address of the subroutine must be within 2K bytes because only 11 bits of the 2-bytes are used for the address

(b) **6**

Timer - 0 Registers:

TH0								TL0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Timer - 1 Registers:

TH1								TL1							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

TMOD Register:

Timer 1				Timer 0			
Gate	C/T	M1	M0	Gate	C/T	M1	M0

SUNIL KUMAR G R, ASST. PROF., KSIT, BENGALURU

TCON: TIMER/COUNTER CONTROL REGISTER							
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Course In-charge

Module Coordinator

HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
III SESSIONAL TEST QUESTION PAPER 2020 – 21 EVEN SEMESTER

SET – A

USN | | | | | | | | | | |

Degree : B.E
Branch : Electronics & Communication Engg.
Course Title : MICROCONTROLLER
Duration : 90 Minutes

Semester : IV A & B
Course Code : 18EC46
Date : 7/8/2021
Max Marks : 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	CO mapping	K-Level
	PART-A			
1(a)	**Explain** the interrupt vector table and IE register.	6	CO5	Applying K-3
(b)	With a neat interfacing diagram, **construct** an ALP to interface an LCD display to display message MICROCONTROLLER on it	6	CO5	Applying K-3
(C)	With a neat interfacing diagram, **construct** an ALP to program 8051 to rotate a stepper motor in clockwise direction continuously.	6	CO5	Applying K-3
	OR			
2(a)	**List** the steps in executing an Interrupt.	6	CO5	Applying K-3
(b)	With a neat interfacing diagram, **construct** an ALP to interface an LCD display to display KSIT in first line and BENGALURU in second line.	6	CO5	Applying K-3
(C)	With a neat interfacing diagram, **construct** an ALP to program 8051 to rotate a stepper motor in anticlockwise direction continuously.	6	CO5	Applying K-3
	PART-B			
3(a)	Assume XTAL = 11.0592 MHz. **Write** a program to generate a square wave of 50Hz frequency on pin P2.3.	6	CO4	Applying K-3
(b)	**Write** an 8051 C program to transfer the message "INDIA" serially at 9600 baud rate continuously.	6	CO4	Applying K-3
	OR			
4(a)	Assume XTAL = 11.0592 MHz. What value do we need to load into the timer's registers if we want to have a time delay of 5 msec? **Write** the program for Timer 0 to create a pulse width of 5 msec on P2.3.	6	CO4	Applying K-3
(b)	**Write** an ALP to transfer the message "YES" serially at 4800 baud, continuously.	6	CO4	Applying K-3

Course in charge | Module Coordinator | HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

III SESSIONAL TEST Scheme 2020 – 21 EVEN SEMESTER

SET – A

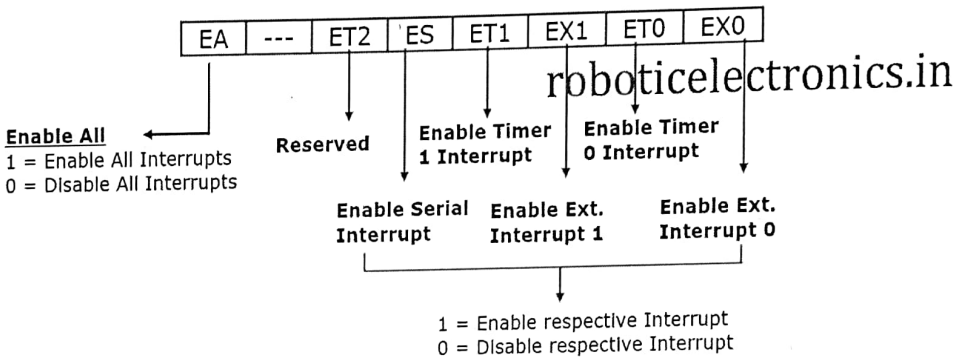
Degree	:	**BE**	**Semester** :	**IV A & B**
Branch	:	**Electronics and Communication Engg**	**Course Code** :	**18EC46**
Course Title	:	**Microcontroller**	**Date** :	**7/8/2021**
Duration	:	**90 Minutes**	**Max Marks** :	**30**

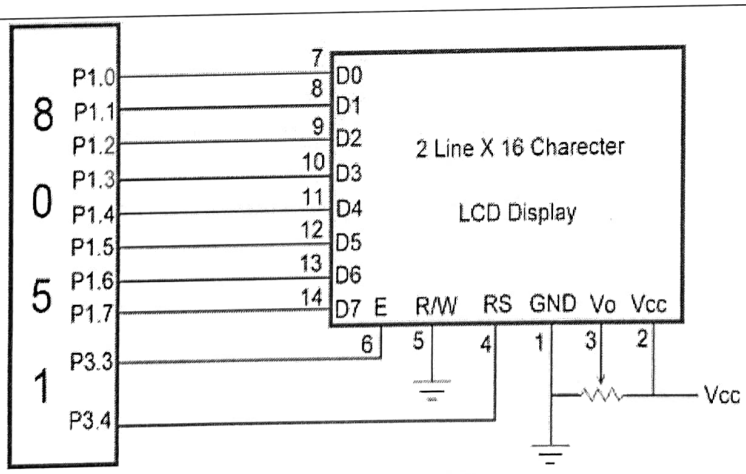
Note: Answer ONE full question from each part.

Q No.	Question	Marks
1 (a)		6
(b)		6

Interrupt	ROM Location (Hex)	Pin	Flag Clearing
Reset	0000	9	Auto
External hardware interrupt 0 (INT0)	0003	P3.2 (12)	Auto
Timer 0 interrupt (TF0)	000B		Auto
External hardware interrupt 1 (INT1)	0013	P3.3 (13)	Auto
Timer 1 interrupt (TF1)	001B		Auto
Serial COM interrupt (RI and TI)	0023		Programmer clears it.

IE - Interrupt Enable (SFR) [Bit-Addressable As IE.7 to IE.0]

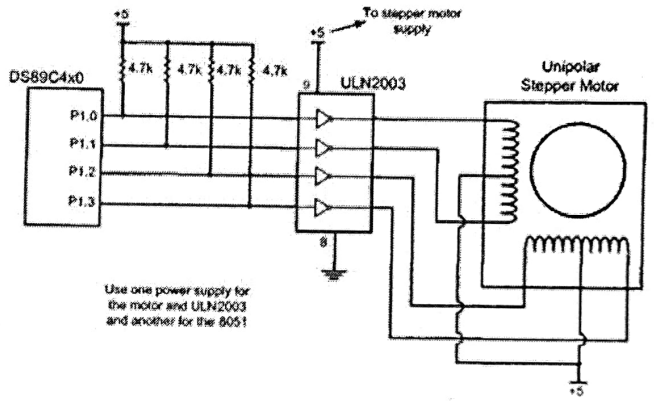




```
ORG 0000H
        MOV A,#38H
        ACALL COMMAND
        ACALL DELAY
        MOV A,#01H
        ACALL COMMAND
        ACALL DELAY
        MOV A,#80H
        ACALL COMMAND
        ACALL DELAY
        MOV A,#'M'
        ACALL DATA
        ACALL DELAY
        MOV A,#'I'
        ACALL DATA
        ACALL DELAY
        MOV A,#'C'
        ACALL DATA
        ACALL DELAY
        .
        .
        MOV A,#'R'
        ACALL DATA
        ACALL DELAY
END

COMMAND:
CLR P3.4
MOV P1,A
SET P3.3
ACALL DELAY
CLR P3.3
RET

DATA:
SETB P3.4
MOV P1,A
SET P3.3
ACALL DELAY
CLR P3.3
RET

DELAY:
        MOV R2,#10H
BACK:   MOV R3,#0FFH
STAY:   DJNZ R3, STAY
        DJNZ R2,BACK
RET
```

(C)

```
org 0000h
        mov p1, #0ffh
        mov a, #77h
        mov p2, a
turn:   rr a
        acall delay
        mov p2, a
        sjmp turn

delay: mov R2, #255
h1:    mov R3, #255
h2:    djnz R3, h2
       djnz R2, h1
       ret
end
```



6

2 (a)

Upon activation of an interrupt, the MC goes through the following steps:

1. 8051 finishes the instruction it is executing and saves the address of the next instruction (PC) on the stack
2. It also saves the current status of all the interrupts internally (not on the stack)
3. It jumps to a fixed location in memory called the interrupt vector table that holds the address of the interrupt service routine (ISR)
4. The MC gets the address of the ISR from the interrupt vector table and jumps to it. It starts to execute ISR until it reaches the last instruction of the subroutine, which is RETI (return from interrupt)
5. Upon executing the RETI instruction, the MC returns to the place where it was interrupted. First it gets the PC address from the stack by popping the two bytes of the stack into the PC; then it starts to execute from that address

6

(b)

```
ORG 0000H
        MOV A,#38H
        ACALL COMMAND
        ACALL DELAY
        MOV A,#01H
        ACALL COMMAND
        ACALL DELAY
        MOV A,#80H
        ACALL COMMAND
        ACALL DELAY
        MOV A,#'K'
        ACALL DATA
        ACALL DELAY
        MOV A,#'S'
        ACALL DATA
        ACALL DELAY
        MOV A,#'I'
        ACALL DATA
        ACALL DELAY
        .
        .
        MOV A,#'U'
        ACALL DATA
        ACALL DELAY
END

COMMAND:
CLR P3.4
MOV P1,A
SET P3.3
ACALL DELAY
CLR P3.3
RET

DATA:
SETB P3.4
MOV P1,A
SET P3.3
ACALL DELAY
CLR P3.3
RET

DELAY:
        MOV R2,#10H
BACK:   MOV R3,#0FFH
STAY:   DJNZ R3, STAY
        DJNZ R2,BACK
RET
```

6

(C)

```
org 0000h
      mov p1, #0ffh
      mov a, #77h
      mov p2, a
turn: rl a
      acall delay
      mov p2, a
      sjmp turn

delay: mov R2, #255
h1:    mov R3, #255
h2:    djnz R3, h2
       djnz R2, h1
       ret
end
```

6

3 (a)

```
ORG 0000H
            MOV TMOD, #10H
REPEAT:MOV TH1, #0DBH
            MOV TL1, #0FFH
            SETB TR1
STAY:JNB TF1, STAY
            CPL P2.3
            CLR TR1
            CLR TF1
            SJMP REPEAT
END
```

Given, fc = 11.0592 MHz
Time Period, t= 1/11.0592 MHz = 0.0904 µsec
Machine Cycle Period, T = 0.0904 µsec x 12 = 1.085 µsec
To find initial values TH and TL:
F=50Hz, T = 1/50Hz = 20msec, delay=T/2 = 10msec
1. 10msec/1.085 µsec = 9216.589 = 9217
2. 65536 – 9217 = 56319
3. DBFFH
4. TH = DB, & TL = FF

6

(b)	#include<reg51.h>
	Void serial(unsigned char);
	Void main(void)
	{
	TMOD=0x20;
	TH1=0xFD;
	SCON=0x50;
	TR1=1;
	while(1)
	{
	serial('I');
	serial('N');
	serial('D');
	serial('I');
	serial('A');
	}
	}
	Void serial(unsigned char x)
	{
	SBUF=x;
	while(TI==0);
	TI=0;
	}
		6

4 (a)	ORG 0000H
	SET P2.3
	MOV TMOD, #01H
	MOV TL0, #00H
	MOV TH0, #0EEH
	SETB TR0
	STAY: JNB TF0, STAY
	CLR P2.3
	CLR TR0
	CLR TF0
	END
	Given, fc = 11.0592 MHz
	Time Period, t= 1/11.0592 MHz = 0.0904 µsec
	Machine Cycle Period, T = 0.0904 µsec x 12 = 1.085 µsec
	To find initial values TH and TL:
	1. 5msec/1.085 µsec = 4608.29 = 4608D
	2. 65536 – 4608 = 60928D
	3. EE00H
	4. TH0 = EEH and TL0 = 00H – initial value
		6

(b)	ORG 0000H
	MOV TMOD,#20H
	MOV TH1,#-6
	MOV SCON,#50H
	SETB TR1
	AGAIN: MOV A, #"Y"
	ACALL SEND
	MOV A, #"E"
	ACALL SEND
	MOV A, #"S"
	ACALL SEND
	SJMP AGAIN
	SEND: MOV SBUF,A
	HERE: JNB TI, HERE
	CLR TI
	RET
		6

Course in charge **Module Coordinator** **HOD/ECE**

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
I SESSIONAL TEST QUESTION PAPER 2020 – 21 EVEN SEMESTER

USN | | | | | | | | | | |

Set B

Degree : B.E
Branch : Electronics & Communication Engg
Subject Title : MICROCONTROLLER
Duration : 90 Minutes

Semester : IV A & B
Subject Code : 18EC46
Date : 26.05.2021
Max Marks : 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	CO mapping	K-Level
	PART-A			
1(a)	**Discuss** the uses of A,B and PSW registers in detail.	6	CO1	K3 Applying
(b)	**Explain** internal RAM structure of 8051 microcontroller.	6	CO1	K3 Applying
(c)	**Explain** the interfacing of 16K EPROM and 8K RAM to 8051.	6	CO1	K3 Applying
	OR			
2(a)	**Chart out** the Difference between Microprocessor and Microcontroller and also brief about embedded system	6	CO1	K3 Applying
(b)	**Sketch** the neat diagram of 8051 PIN-OUT and explain the following pins i)ALE ii) $\overline{PSEN}$ iii) $\overline{EA}$ iv)RST v) RD vi) $\overline{WR}$	6	CO1	K3 Applying
(c)	**Explain** the Interfacing of 4k bytes RAM and 8k bytes ROM to 8051 microcontroller	6	CO1	K3 Applying
	PART-B			
3(a)	**Explain** the addressing modes of 8051 microcontroller with example.	6	CO2	K3 Applying
(b)	**Explain** the following instructions with an example. i)MOVC A,@A+DPTR ii)XCHD A,@R0 iii)XCH A,81h iv) MUL AB	6	CO2	K3 Applying
	OR			

4(a)	**Explain** the following instructions, also find out the result of each instruction and specify RAM location if its stored in RAM.
	MOV DPTR,#6789h
	MOV A,DPH
	ADD A,DPL
	MOV R0,A
	MOV @R0,A
	MOVX @DPTR,A
		6	CO2	K3 Applying

(b)	**Make use of** 8051 instructions check the correctness of the following instruction. If wrong correct them. i)MOV R5,R7 ii) ADD B,A iii) MOV A,@R3 iv)MOVX A,@R0 v)XCH @R0,A vi)DIV A,B	6	CO2	K3 Applying

Course in charge Module Coordinator Signature of HOD

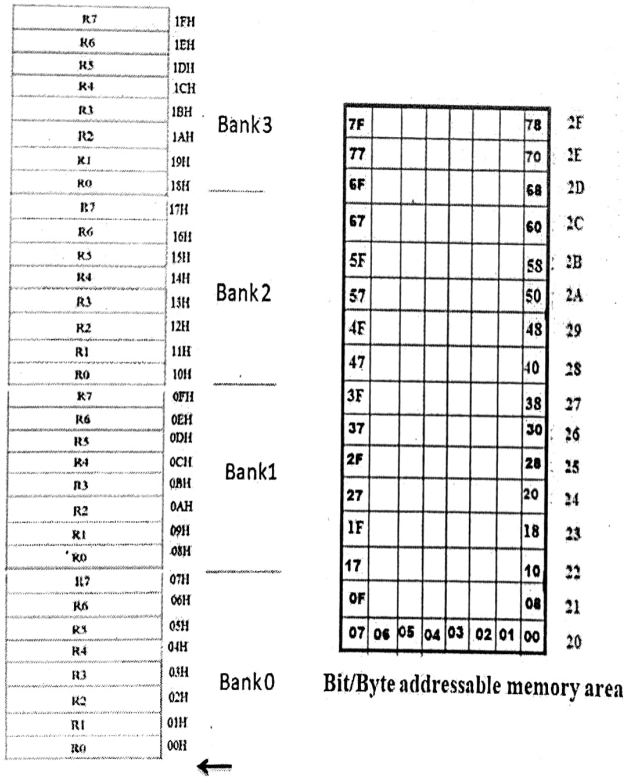
K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

I SESSIONAL TEST scheme 2020 – 21 EVEN SEMESTER

SET – B

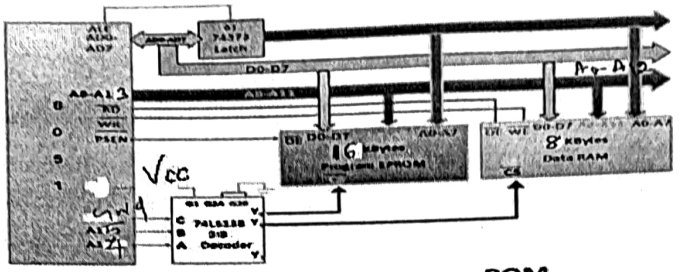
Degree	: **BE**	**Semester :**	**IV A & B**
Branch	: **Electronics and Communication Engg**	**Course Code :**	**18EC46**
Course Title	: **Microcontroller**	**Date :**	**26/05/21**
Duration	: **90 Minutes**	**Max Marks :**	**30**

Note: Answer ONE full question from each part.

Q No.	Question	Marks
1 (a)	**Accumulator** (Register A*): *Address-E0H* It is an 8-bit register used for many operations including addition, subtraction, multiplication, division, and Boolean bit manipulations. This is also used for all data transfers between 8051 and any external memory. It can also be used as a general purpose register. The results obtained from arithmetic and logical instructions are always stored in Accumulator. **Register B*:** *Address-F0H* It is an 8-bit register specially used for direct multiplication and division operation with Accumulator. Both A and B registers are called **math registers** in 8051 family. It can also be used as a general-purpose storage location with its direct address (F0H). **PSW** 7 6 5 4 3 2 1 0 CY AC F0 RS1 RS0 OV – P D7 D6 D5 D4 D3 D2 D1 D0	6
(b)		6

(C)

Interface 16K byte EPROM and 8K byte RAM to 8051



Memory Map - Program ROM

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
Starting Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
2nd Location	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001H
.									.								.
Ending Address	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

Memory Map - Data RAM

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
Starting Address	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	2000H
2nd Location	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	2001H
.									.								.
Ending Address	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

6

2 (a)

	MICROPROCESSOR	MICROCONTROLLER
1	MP have many operational codes for moving data from external memory to the CPU	MC may have one or two
2	MP may have one or two bit handling instructions	MC will have many
3	Less multifunction pins on IC	Many multifunction pins on IC
4	MP takes many instructions to read and write data from external memory	MC takes few instructions to read and write data from external memory
5	Generally higher core clock frequency	Generally lower core clock frequency
6	High performance pipelined CPU Architecture	Low performance pipelined CPU Architecture
7	General purpose processor	Application specific single chip solution

6

(b)

PSEN : This is an output pin. PSEN stands for "program store enable." In an 8051-based system in which an external ROM holds the program code, this pin is connected to the OE (output Enable)pin of the ROM. This pin is used to enable external program memory. If we use an external ROM for storing the program, then logic 0 appears on it, which indicates Micro controller to read
data from the memory

EA : The 8051 family members, such as the 8751/52, 89C51/52, or DS89C4xO, all come with on-chip ROM to store programs. In such cases, the EA pin is connected to Vcc. For family.

ALE stands for **Address Latch Enable**. It is input, active-high pin. This pin is used to distinguish between memory chips when multiple memory chips are used. It is also used to de-multiplex the multiplexed address and data signals available at port 0.

P3.0---RXD : Serial communication Receiver terminal

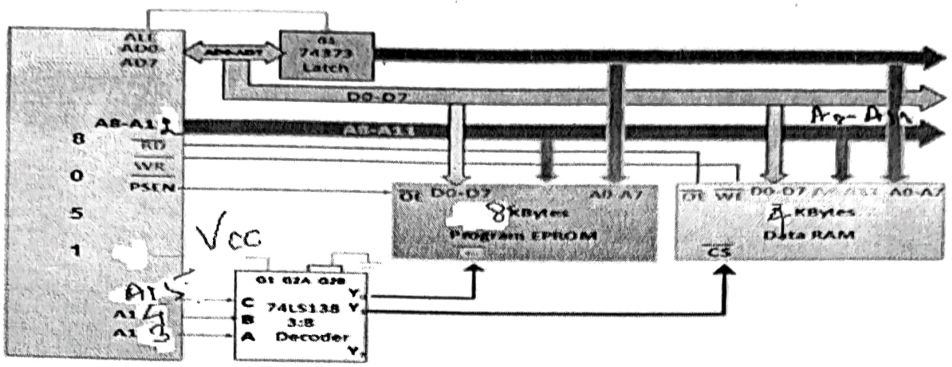
P3.1---TXD : Serial communication Transmitter terminal

RST-Reset the microcontroller and load the program counter by 0000

6

(C)

Interface 16K byte EPROM and 8K byte RAM to 8051



Memory Map - Program ROM

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
Starting Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
2nd Location	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001H
.									.								.
.									.								.
Ending Address	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1FFFH

Memory Map - Data RAM

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
Starting Address	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	2000H
2nd Location	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	2001H
.									.								.
.									.								.
Ending Address	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

6

---

3 (a)

There are 5 addressing modes: i) immediate, ii) register, iii) direct, iv) register indirect and v) indexed: Examples: i) MOV A, #25H, ii) MOV A, R0, iii) MOV R0, 40H, iv) MOV A, @R0, v) MOVC A, @A+DPTR

6

(b)

i)MOVC A,@A+DPTR ii)XCHD A,@R0 iii)XCH A,81h iv) MUL AB

i) The address for the operand is the sum of contents of DPTR and Accumulator.

ii)Exchange Acc lower nibble with lower nibble of address pointed by R0

iii)Exchange data between Acc with address pointed by 81h.

iv)Multiply A with B ,result lower byte in A, and higher byte in B

6

---

4 (a)

```
MOV DPTR,#6789h   ; DPTR =6789h
MOV A,DPH         ; A=67h
ADD A,DPL         ; A=0F0h
MOV R0,A          ; R0=0F0h
MOV @R0,A         ; [0F0h]=F0h
MOVX @DPTR,A      ;x:[6789h]=0F0h
```

6

(b)

i)MOV R5,R7 ii) ADD B,A iii) MOV A,@R3 iv)MOVX A,@R0 v)XCH @R0,A vi)DIV A,B

i)Wrong ,should be MOV R5,A ii)Wrong bec destination must be ACC iii)Wrong ,because R0 and R1 must be address pointer iv)Wrong, because R0 cant be external pointer v)Wrong because A should be ACC vi)Wrong because syntax is DIV AB

6

Course in charge Module Coordinator HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
II SESSIONAL TEST QUESTION PAPER 2020 – 21 EVEN SEMESTER

SET – B

USN | | | | | | | | | | |

Degree : B.E
Branch : Electronics and Communication Engg
Course Title : Microcontroller
Duration : 90 Minutes

Semester : IV A & B
Course Code : 18EC46
Date : 30/06/21
Max Marks : 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	CO mapping	K-Level
	PART-A			
1(a)	**Write** an ALP to rotate the content of A=F8h left by five positions and rotate right by two positions then store final result in B register and show the manual calculation of value of B.	6	CO3	K3
(b)	**Write** an ALP to Count number of one's and zero's in an 8bit data using 1) CALL instruction and 2) JUMP instruction	6	CO3	K3
(C)	**Explain** with neat block diagram the stack pointer position changes during subroutine execution using CALL and RET instruction.	6	CO3	K3
	OR			
2(a)	**Write** an ALP to find the value of expression K=[(P+Q) +45h]. Values of P and Q are stored in the internal memory locations 22h and 23h respectively. Store the result in 24h.	6	CO3	K3
(b)	**Write** an ALP to find the sum of ten 8bit numbers stored in the internal memory alternate addresses. And block of data is stored in locations 30h, 32h, 34h etc. finally store the 16-bit sum at locations 45h and 46h.	6	CO3	K3
(C)	With a neat interface circuit diagram, **write** an ALP to read the Lower nibble of port P1 to be displayed on LEDs, which are connected to Upper nibble of port P2.	6	CO3	K3
	PART-B			
3(a)	**What** is the difference between bit addressable and byte addressable in Microcontroller, explain them using suitable examples	6	CO2	K3
(b)	**What** are timers and Counters? Explain using suitable block diagram.	6	CO4	K3
	OR			
4(a)	**Explain** the following instructions using suitable examples. i)JC ii)JB iii)JZ iv)CJNE	6	CO2	K3
(b)	How to configure and run the timer1 in mode 1 using one control bit. **What** is the value of TMOD for the above mentioned mode & timer and also explain each bit of TMOD register.	6	CO4	K3

Staff In charge Module Coordinator HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

II SESSIONAL TEST scheme 2020 – 21 EVEN SEMESTER

SET – B

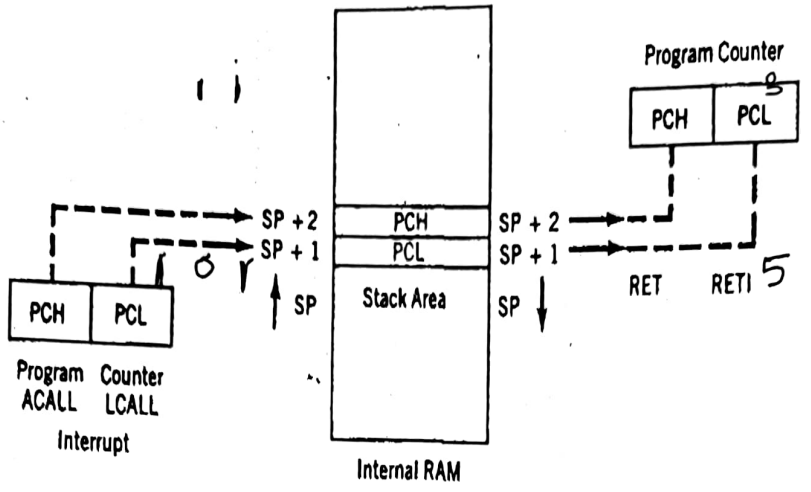
Degree	**: BE**	**Semester :**	**IV A & B**
Branch	**: Electronics and Communication Engg**	**Course Code :**	**18EC46**
Course Title	**: Microcontroller**	**Date :**	**30/06/21**
Duration	**: 90 Minutes**	**Max Marks :**	**30**

Note: Answer ONE full question from each part.

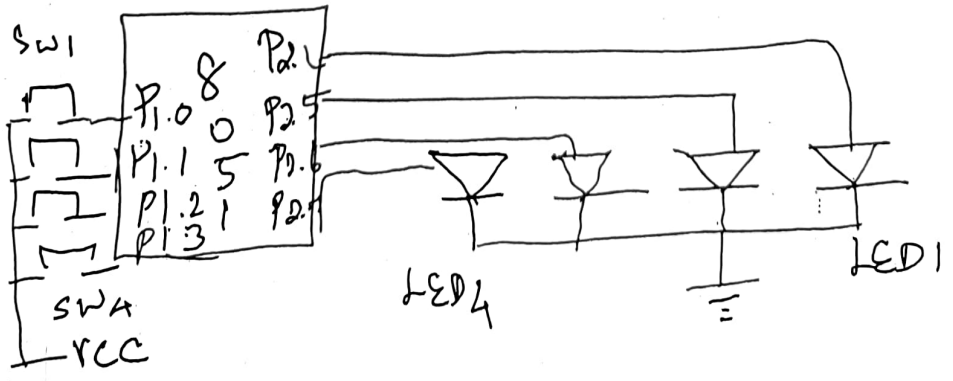
Q No.	Question	Marks

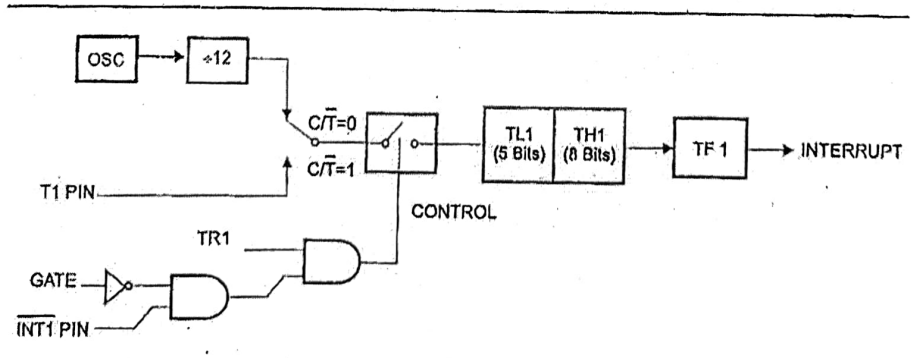
1 (a)	mov a,#0f8h
	mov r7,#05h
	back:rl a
	djnz r7,back
	rr a
	rr a
	mov b,a ; b=c7h
	end
		6

(b)	**Using Call Instructions:**
	mov a,#N
	mov r7,#08h
	call find
	sjmp last
	find: rrc a
	jc ones
	zeros:inc r3
	sjmp next
	ones: inc r4
	next: djnz r7,find
	ret
	last:nop
	end
	Using Jump Instructions
	Mov a,#N
	mov r7,#08h
	back: rrc a
	jc ones
	zeros:inc r3
	sjmp next
	ones: inc r4
	next: djnz r7,back
	end
		6

(C)	Storing and Retrieving the Return Address  	6
2 (a)	mov a,22h ------p add a,23h -------q addc a,#45h ----- k mov 24h,a end	6

(b)	mov r7,#0ah
	mov r0,#30h
	mov a,@r0
	back:inc r0
	inc r0
	mov 0f0h,@r0
	addc a,b
	djnz r7, back
	mov 45h,a
	
	mov a,#00h
	addc a,#00h
	end
		6

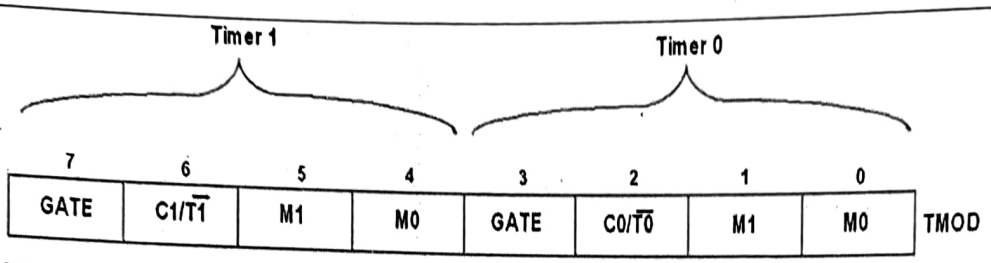
(C)	
	
	Mov p1,#0ffh
	Mov p2,#00h
	Mov p1,#00h
	back:Jb p1,0,led1
	Jb p1.1,led2
	Jb p1.2,led3
		6

	Jb p1.3,led4 Sjmp back Led1:setb p2.4 Nop Clr p2.4 Sjmp back Led2:setb p2.5 Nop Clr p2.5 Sjmp back Led3:setb p2.6 Nop Clr p2.6 Sjmp back Led4:setb p2.7 Nop Clr p2.7 Sjmp back end	
3 (a)	In Byte addressable we can only access the data by byte by byte i.e whole bunch of 8 bits. but in bit addressable addresses we can access or manipulate each bit individually. In 8051 memory map, 4 register banks RB0,RB1,RB2 and RB3(each contains 8 registers of 8 bit R0,R1,R2.....R7 from RAM address 0x00 to 0x1F) and scratch pad area from 0x30 to 0x7F is byte addressable. From RAM address 0x20 to 0x2F and some SFR's (Special Function Registers) are bit addressable. Mov b,#20h Setb 01h	6
(b)	8051 microcontrollers have two timers/counters which work on the clock frequency. Timer/counter can be used for time delay generation, counting external events, etc. **MODE 0**  **Fig. 12.16 Timer/counter 1 mode 0 : 13-bit counter**	6
4 (a)	i)JC ii)JB iii)JZ iv)CJNE i)rrc a jc l1 ii)subb a,b jb l1	6

iii)dec a
jz l1

iii)cjne a,#20h,l1

(b)



Mov Tmod,#10h

M1	M0	Mode	Operation
0	0	0 (13-bit timer mode)	13-bit timer/counter, 8-bit of THx & 5-bit of TLx
0	1	1 (16-bit timer mode)	16-bit timer/counter, THx cascaded with TLx
1	0	2 (8-bit auto-reload mode)	8-bit timer/counter (auto-reload mode), TLx reload with the value held by THx each time TLx overflow
1	1	3 (split timer mode)	Split the 16-bit timer into two 8-bit timers i.e. THx and TLx like two 8-bit timer

6

Course in charge

Module Coordinator

HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
III SESSIONAL TEST QUESTION PAPER 2020 – 21 EVEN SEMESTER

SET – B

USN

Degree	: B.E	Semester	: IV A & B
Branch	: Electronics & Communication Engg.	Course Code	: 18EC46
Course Title	: MICROCONTROLLER	Date	: 7/8/2021
Duration	: 90 Minutes	Max Marks	: 30

Note: Answer ONE full question from each part.

Q No.	Question	Marks	CO mapping	K-Level
	PART-A			
1(a)	List the steps in executing an Interrupt.	6	CO5	K-3
(b)	With a neat interfacing diagram, **construct** an ALP to interface an LCD display to display a message on it	6	CO5	K-3
(C)	With a neat interfacing diagram, **construct** an ALP to program 8051 to rotate a stepper motor in Anti-clockwise directions.	6	CO5	K-3
	OR			
2(a)	**Explain** the interrupt vector table and IE register.	6	CO5	K-3
(b)	With a neat interfacing diagram, **construct** an ALP to interface an LCD display 'VTU' to display a message on it	6	CO5	K-3
(C)	With a neat interfacing diagram, **construct** an ALP to program 8051 to rotate a stepper motor in clockwise directions.	6	CO5	K-3
	PART-B			
3(a)	Assume XTAL = 11.0592 MHz. **Write** a program to generate a square wave of 50Hz frequency on pin P2.3.	6	CO4	K-3
(b)	**Write** an 8051 C program to transfer the message "KSIT" serially at 9600 baud rate continuously.	6	CO4	K-3
	OR			
4(a)	Assume XTAL = 11.0592 MHz. What value do we need to load into the timer's registers if we want to have a time delay of 5 msec? **Write** the program for Timer 0 to create a pulse width of 5 msec on P2.3.	6	CO4	K-3
(b)	**Write** an ALP to transfer the message "YES" serially at 4800 baud, continuously.	6	CO4	K-3

Course in charge

Module Coordinator

HOD/ECE

Selected

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109
III SESSIONAL TEST scheme 2020 – 21 EVEN SEMESTER

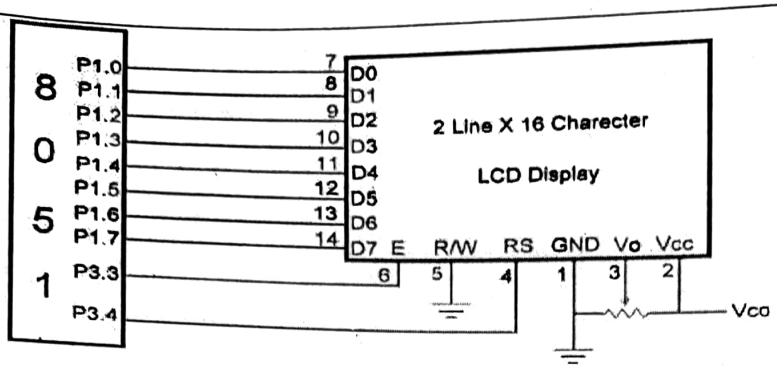
SET – B

Degree	:	**BE**	**Semester**	:	**IV A & B**
Branch	:	**Electronics and Communication Engg**	**Course Code**	:	**18EC46**
Course Title	:	**Microcontroller**	**Date**	:	**30/06/21**
Duration	:	**90 Minutes**	**Max Marks**	:	**30**

Note: Answer ONE full question from each part.

Q No.	Question	Marks
1 (a)	Upon activation of an interrupt, the MC goes through the following steps: 1. 8051 finishes the instruction it is executing and saves the address of the next instruction (PC) on the stack 2. It also saves the current status of all the interrupts internally (not on the stack) 3. It jumps to a fixed location in memory called the interrupt vector table that holds the address of the interrupt service routine (ISR) 4. The MC gets the address of the ISR from the interrupt vector table and jumps to it. It starts to execute ISR until it reaches the last instruction of the subroutine, which is RETI (return from interrupt) 5. Upon executing the RETI instruction, the MC returns to the place where it was interrupted. First it gets the PC address from the stack by popping the two bytes of the stack into the PC; then it starts to execute from that address	6

(b)	ORG 0000H
	MOV A,#38H
	ACALL COMMAND
	MOV A,#01H
	ACALL COMMAND
	MOV A,#80H
	ACALL COMMAND
	MOV A,#'K'
	ACALL DATA
	MOV A,#'S'
	ACALL DATA
	MOV A,#'I'
	ACALL DATA
	MOV A,#'T'
	ACALL DATA
	DATA:CLR P3.4
	MOV P2,A
	CLR P3.4
	ACALL DELAY
	MOV P3.4
	RET
	DATA:SETB P3.4
	MOV P2,A
	CLR P3.4
	ACALL DELAY
	MOV P3.4
	RET
	DELAY:MOV R7,#255
	HERE:DJNZ R7,HERE
	END
		6



(C)

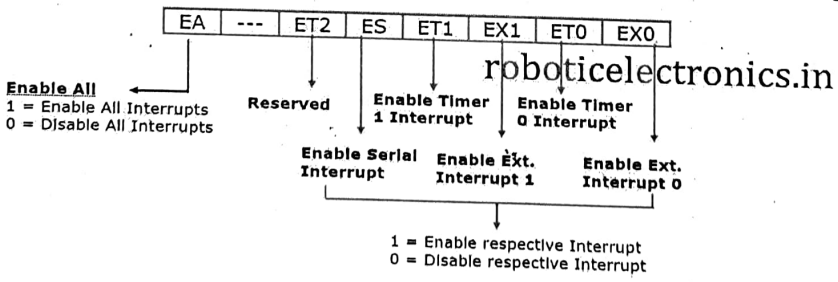
```
org 0000h
mov p1, #0ffh
mov a, #77h
mov p2, a
turn: rl a
acall delay
mov p2, a
sjmp turn
delay: mov R2, #255
h1: mov R3, #255
h2: djnz R3, h2
djnz R2, h1
ret
end
```

6

2 (a)

Interrupt	ROM Location (Hex)	Pin	Flag Clearing
Reset	0000	9	Auto
External hardware interrupt 0 (INT0)	0003	P3.2 (12)	Auto
Timer 0 interrupt (TF0)	000B		Auto
External hardware interrupt 1 (INT1)	0013	P3.3 (13)	Auto
Timer 1 interrupt (TF1)	001B		Auto
Serial COM interrupt (RI and TI)	0023		Programmer clears it.

IE - Interrupt Enable (SFR) [Bit-Addressable As IE.7 to IE.0]

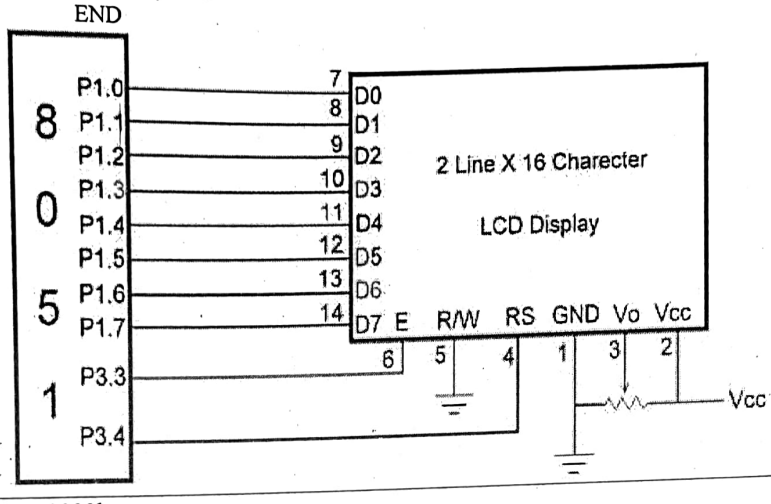


6

(b)

```
ORG 0000H
MOV A,#38H
ACALL COMMAND
MOV A,#01H
ACALL COMMAND
MOV A,#80H
ACALL COMMAND
MOV A,#'V'
ACALL DATA
MOV A,#'T'
```

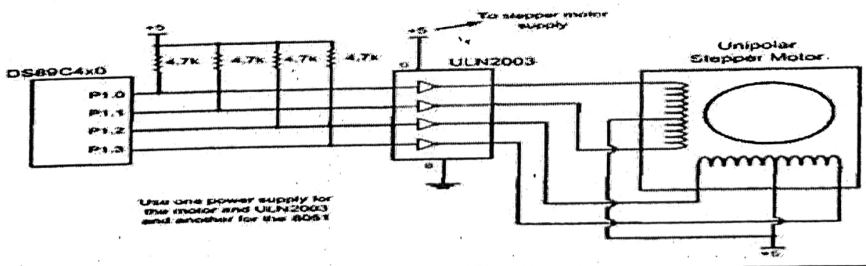
```
ACALL DATA
MOV A,#'U'
ACALL DATA
DATA:CLR P3.4
        MOV P2,A
        CLR P3.4
        ACALL DELAY
        MOV P3.4
        RET
DATA:SETB P3.4
        MOV P2,A
        CLR P3.4
        ACALL DELAY
        MOV P3.4
        RET
DELAY:MOV R7,#255
HERE:DJNZ R7,HERE
        END
```



(C)

```
org 0000h
mov p1, #0ffh
mov a, #77h
mov p2, a
turn: rr a
acall delay
mov p2, a
sjmp turn
delay: mov R2, #255
h1: mov R3, #255
h2: djnz R3, h2
djnz R2, h1
ret
end
```

6



3 (a)

```
ORG 0000H
MOV TMOD, #10H
REPEAT:MOV TH1, #0DBH
MOV TL1, #0FFH
SETB TR1
STAY: JNB TF1, STAY
```

6

	CPL P2.3 CLR TR1 CLR TF1 SJMP REPEAT END	

(b)	#include<reg51.h>
	Void serial(unsigned char);
	Void main(void)
	{
	TMOD=0x20;
	TH1=0xFD;
	SCON=0x50;
	TR1=1;
	while(1)
	{
	serial('K');
	serial('S');
	serial('I');
	serial('T');
	}
	}
	Void serial(unsigned char x)
	{
	SBUF=x;
	while(TI==0);
	TI=0;
	}
		6

4 (a)	ORG 0000H
	SET P2.3
	MOV TMOD, #01H
	MOV TL0, #00H
	MOV TH0, #0EEH
	SETB TR0
	STAY: JNB TF0, STAY
	CLR P2.3
	CLR TR0
	CLR TF0
	END
		6

(b)	ORG 0000H
	MOV TMOD,#20H
	MOV TH1,#-6
	MOV SCON,#50H
	SETB TR1
	AGAIN: MOV A, #"Y"
	ACALL SEND
	MOV A, #"E"
	ACALL SEND
	MOV A, #"S"
	ACALL SEND
	SJMP AGAIN
	SEND: MOV SBUF,A
	HERE: JNB TI, HERE
	CLR TI
	RET
	END
		6

Course in charge Module Coordinator HOD-ECE

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

Course: Microcontroller | **sem: IV** | **sec: A**

Sl. No.	USN No.	Name	IA1	IA2	IA3	A1	A2	A3	Average Assignment	Average of three IA's	Final IA(Assignment+IA)
1	1KS19EC001	ABHILASH A S	24	23	28	10	10	10	10	25	35
2	1KS19EC002	ABHISHEK CHANDRESH	23	23	27	10	10	10	10	25	35
3	1KS19EC003	AISHWARYA BASAVARAJ KEMBAVI	23	23	29	10	10	10	10	25	35
4	1KS19EC004	AISHWARYA M G	25	23	25	10	10	10	10	25	35
5	1KS19EC005	AKSHAY KUMAR D	23	23	24	10	10	10	10	24	34
6	1KS19EC006	AKSHITHA	25	23	29	10	10	10	10	26	36
7	1KS19EC007	AMRUTA	24	22	28	10	10	10	10	25	35
8	1KS19EC008	AMULYA R	25	27	23	10	10	10	10	25	35
9	1KS19EC009	ANITHA S	25	26	29	10	10	10	10	27	37
10	1KS19EC010	ANJALI Y J	27	28	28	10	10	10	10	28	38
11	1KS19EC011	ARCHANA YADAV M	25	23	24	10	10	10	10	24	34
12	1KS19EC012	ASHRITHA R	22	28	25	10	10	10	10	25	35
13	1KS19EC014	BHAVANA S	24	23	27	10	10	10	10	25	35
14	1KS19EC015	CHAITRA P	24	27	27	10	10	10	10	26	36
15	1KS19EC016	CHANDAN RAJ Y	25	28	25	10	10	10	10	26	36
16	1KS19EC017	CHANDANA.L	22	23	26	10	10	10	10	24	34
17	1KS19EC018	CHENNREDDY RAJASEKHAR	24	22	24	10	10	10	10	24	34
18	1KS19EC019	CHIRANTHANA YOGANANDA K	22	25	24	10	10	10	10	24	34
19	1KS19EC020	D NAYAN	24	23	27	10	10	10	10	25	35
20	1KS19EC021	DANESH RAJU V	23	23	28	10	10	10	10	25	35
21	1KS19EC022	DAVINO JOSEPH	23	28	27	10	10	10	10	26	36
22	1KS19EC023	DHANYA SUKANTH B K	23	26	26	10	10	10	10	25	35
23	1KS19EC024	DHEEMANTH K N	25	23	24	10	10	10	10	24	34
24	1KS19EC025	DISHA SHIVANI	24	23	24	10	10	10	10	24	34
25	1KS19EC027	GAYATHRI P K	23	26	26	10	10	10	10	25	35
26	1KS19EC028	GAYATHRI R WARRIER	26	25	27	10	10	10	10	26	36
27	1KS19EC029	GONUGUNTLA SAI SIDDARTHA	23	22	24	10	10	10	10	23	33
28	1KS19EC030	GOWRI S NADIGER	25	24	29	10	10	10	10	26	36
29	1KS19EC031	HARSHA R	20	22	25	10	10	10	10	23	33
30	1KS19EC032	HARSHITHA B Y	23	21	24	10	10	10	10	23	33
31	1KS19EC033	HEMANTH.R.PATIL	23	21	27	10	10	10	10	24	34
32	1KS19EC035	JAGRUTI PAI	26	29	28	10	10	10	10	28	38
33	1KS19EC036	JAYANTH M B	24	24	26	10	10	10	10	25	35
34	1KS19EC037	KAMMA MANUBOLU MANOGNA	20	23	29	10	10	10	10	24	34
35	1KS19EC038	KARTHIK K	23	23	24	10	10	10	10	24	34
36	1KS19EC039	KASHYAP.P	22	28	26	10	10	10	10	26	36
37	1KS19EC040	KRUPA.A	25	20	25	10	10	10	10	24	34
38	1KS19EC041	KRUTHI K S	24	26	26	10	10	10	10	26	36
39	1KS19EC042	LAKSHMAN KUMARA B	25	22	27	10	10	10	10	25	35
40	1KS19EC043	LIKITHA.H	25	28	28	10	10	10	10	27	37
41	1KS19EC044	M LOKESHWARI	25	24	29	10	10	10	10	26	36
42	1KS19EC045	MANU N KANDRA	25	22	29	10	10	10	10	26	36
43	1KS19EC046	MEGHANA H P	25	23	24	10	10	10	10	24	34

44	1KS19EC047	MOHAMMAD RAKHEEB M R	25	26	22	10	10	10	10	25	35
45	1KS19EC048	MOHITH KUMAR G	23	27	24	10	10	10	10	25	35
46	1KS19EC049	MONIKA V ARYA	24	26	25	10	10	10	10	25	35
47	1KS19EC050	MONISHA.B.K	25	26	26	10	10	10	10	26	36
48	1KS19EC051	N ANILA	25	28	26	10	10	10	10	27	37
49	1KS19EC052	NIDHI S	23	20	27	10	10	10	10	24	34
50	1KS19EC053	NISARGA K	22	19	24	10	10	10	10	22	32
51	1KS19EC054	NITHIN D	24	27	23	10	10	10	10	25	35
52	1KS19EC055	PAVAN KUMAR G R	25	24	24	10	10	10	10	25	35
53	1KS19EC056	POKURI MOUNIKA	19	23	26	10	10	10	10	23	33
54	1KS19EC057	POOJA S P	25	24	26	10	10	10	10	25	35
55	1KS19EC058	PRADEEP GADED	24	24	23	10	10	10	10	24	34
56	1KS19EC059	PRAKASH CHEGORE	25	24	24	10	10	10	10	25	35
57	1KS19EC061	PRASHANTH.S.K	26	24	25	10	10	10	10	25	35
58	1KS19EC062	PRAVEEN KUMAR N	25	24	23	10	10	10	10	24	34
59	1KS19EC063	PREETHAM G H	23	24	24	10	10	10	10	24	34
60	1KS19EC064	PRIYANKA K	25	27	26	10	10	10	10	26	36
61	1KS19EC065	RADHA KRISHNA L	25	24	25	10	10	10	10	25	35
62	1KS19EC066	RAJALAKSHMI S	27	27	22	10	10	10	10	26	36

K. S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

Department of Electronics and Communication

CHALLENGING QUESTIONS

Course Title: MICROCONTROLLER Course Code: 18EC46

1. Write an ALP to find LCM of two 8-bit numbers.
2. Write an ALP to find GCD of two 8-bit numbers.
3. Write an ALP to generate Fibonacci series.
4. Write an ALP to check whether the given number is prime or not?
5. Write an ALP to check whether the given 8-bit number is a Bit-wise Palindrome or not
6. Write an ALP to check whether the given word is a Palindrome or not?

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE - 560109

DEARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING AND LEARNING

PEDAGOGY REPORT

Academic Year	2020-21 (Even)
Name of the Faculty	Mr. Sunil Kumar G R
Course Name /Code	Microcontroller/18EC46
Semester/Section	IV 'A'
Activity Name	Online Quiz
Topic Covered	Basics Concepts ofMicrocontroller
Date	13/05/2021
No. of Participants	56
Objectives/Goals	To get familiar with Microcontroller basic concepts
ICT Used	Google Forms
Appropriate Method/Instructional materials/Exam Questions Faculty covered the basic concepts of microcontroller, and students were asked to attend the quiz and give their responses through Google Forms.	
Relevant PO's	1,12
Significance of Results/Outcomes	The activity improved student' concepts of Microcontroller.
Reflective Critique	Students fared well with a score of 8.8 out of 10.
Proofs (Photographs/Videos/Reports/Charts/Models): The below link gives the detail of the responses received for the quiz and how they have fared well in the quiz. **https://docs.google.com/forms/d/14rZxRatxFsceeMfKk9ufLRUhhIcTj-aPXE19BShCzFM/edit**	

Signature of Course In charge

Signature of HOD/ECE

K. S. INSTITUTE OF TECHNOLOGY, BANGALORE – 560109

Department of Electronics and Communication

QUESTION BANK

Course Title: MICROCONTROLLER Course Code: 18EC46

Module – 1 & 2

1. With neat diagrams explain the architecture of 8051 microcontroller, internal memory and PSW.
2. Differentiate between Microprocessor and Microcontroller.
3. With a neat diagram explain the pin details of 8051 microcontroller.
4. Explain assembler directives and addressing modes of 8051 microcontroller.
5. Explain the following instructions with an example for each: i) MOVC A, @A+DPTR, ii) POP direct, iii) XCHD A, @Ri, iv) DIV AB, v) CPL A
6. Write an ALP to transfer data blocks from external source memory location to external destination memory location.
7. Write an ALP to transfer data blocks from internal source memory location to external destination memory location.
8. Write an ALP to exchange data blocks from external source memory location to external destination memory location.
9. Write an ALP to exchange data blocks from internal source memory location to external destination memory location.

Module – 3

1. Write an ALP to generate Fibonacci series.
2. Write an ALP to check whether the given number is prime or not?
3. Write an ALP to check whether the given 8-bit number is a Bit-wise Palindrome or not
4. Write an ALP to check whether the given word is a Palindrome or not?
5. Write a code to push R0, R1 and R2 of bank-0 onto the stack memory and pop them into R5, R6 and R7 of bank-3.
6. Write a program to store FFH into RAM locations from 50H to 6FH.
7. Write a program to find y where $y = x^2 + 2x + 5$, assume x between 0 to 9.
8. Write a program to find whether the given number is a '2 out of 5' code or not?

Module – 4 & 5

1. Write a program to see whether the given number is divisible by 8 or not?
2. Write a program to find the number of zero's in register R2.
3. Write a program to find the number of positive and negative numbers in an array.
4. Write a program to complement content of accumulator 62500 times.
5. Write an ALP to interface simple switch and LED to I/O ports to switch on/off LED with respect to switch status.
6. Assume XTAL = 11.0592 MHz, write a program to generate a square wave of 2 kHz frequency on pin P1.5.
7. List out the steps to program the 8051 to transfer data serially.
8. Explain the interrupt vector table and IE register.
9. With a neat interfacing diagram, write an ALP to program 8051 to rotate a stepper motor in clockwise and anticlockwise directions.

CBCS SCHEME

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17EC563

Fifth Semester B.E. Degree Examination, July/August 2021
8051 Microcontroller

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions.*

1 a. Explain the architecture of 8051 microcontroller with a neat diagram. **(10 Marks)**
b. Compare microprocessor and microcontroller. **(04 Marks)**
c. Explain the working of port 0 and port 1 with the help of necessary diagram. **(06 Marks)**

2 a. Show the internal memory organization of 8051. **(06 Marks)**
b. Explain the interfacing of external ROM and RAM to 8031 microcontroller with the help of a neat diagram. **(10 Marks)**
c. Explain the addressability and byte addressability with examples. **(04 Marks)**

3 a. Explain the different addressing modes with examples. **(08 Marks)**
b. Explain the following instructions with examples.
i) DJNZ R2, again ii) MOV A, 50h iii) INC R1 iv) DA A **(08 Marks)**
c. Write an ALP to add two 16-bit numbers. **(04 Marks)**

4 a. Write an ALP to transfer the data bytes 10h, 20h, 30h, 40h, 50h to memory locations 60h, 61h, 62h, 63h, 64h without using loops. **(08 Marks)**
b. Explain different rotate instructions with examples. **(08 Marks)**
c. Mention the flags of PSW and its applications in instructions. **(04 Marks)**

5 a. Explain the sequence of events when a call opcode occurs in the program and use of stack with necessary diagram. **(08 Marks)**
b. Write an ALP to find factional of an 8-bit number. The result should be maximum of 8-bit. **(06 Marks)**
c. Write an ALP to add first 10 natural numbers. **(06 Marks)**

6 a. Write an ALP to find smallest number in an array of 10 bytes from location 60h. **(10 Marks)**
b. Show different jump instructions in 8051 with diagram based on range. **(06 Marks)**
c. In the Fig Q6(c), write an ALP to turn on LED when switch is pressed and turn off, LED when switch is not pressed.

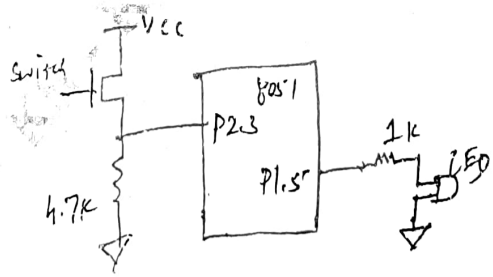

Fig Q6(c) **(04 Marks)**

7 a. Explain the brief the operation of timer in mode 1 and mode 2. Also calculate the maximum delay for both modes if XTAL is 11.0592MHz. **(10 Marks)**

b. Generate a waveform given in Fig Q7(b), if XTAL = 11.0592MHz P1.3 use timer 0 in mode 1.

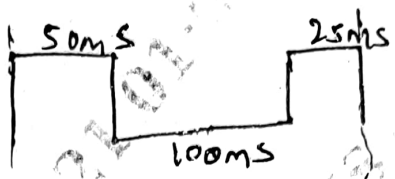

Fig Q7(b) **(10 Marks)**

8 a. Generate a square wave of frequency of 1KHz and 2KHz using timer 1 in mode 2 Assume XTAL = 22MHz. **(10 Marks)**

b. Write an 8051 C program to send two different strings to the serial port. Assuming that SW is connected to pin P2.0, monitor its status and make a decision follows :
SW = 0 : Send your data as BE
SW = 1 : Send your data as VTU
Assume XTAL = 11.0592MHz, baud rate of 9600, 8-bit data, 1 stop bit. **(10 Marks)**

9 a. Two switches are connected to pins P3.2 and P3.3. When a switch is pressed, the correspond lines goes low. Write an assemble language program to
i) Light an LED's connected to port 0 , if first switch is pressed
ii) Light all LED's connected to port 2, if the second switch is pressed **(10 Marks)**

b. Write a C program to create a square wave of 200ms period on pin 2.5. Use timer 0 in mode 2. Assume XTAL = 11.0592MHz. Simultaneously get data from P1.7 and send it to P1.0. **(10 Marks)**

10 a. With a neat diagram, explain interfacing of LCD to 8051. **(06 Marks)**

b. A switch is connected to pin P2.7. Write a assembly language program to monitor the status of SW and perform the following :
i) If SW = 0, the stepper motor moves clockwise
ii) If SW = 1, the stepper motor moves counter clockwise. **(08 Marks)**

c. With the neat diagram, explain the interfacing of ADC 0804 to 8051 Microcontroller **(06 Marks)**

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17EC563

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
8051 Microcontroller

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Differentiate between Microprocessor and Microcontroller with respect to their architecture and instructions. **(06 Marks)**

b. Explain the Oscillator circuit and machine cycle of 8051 Microcontroller. **(06 Marks)**

c. Explain the Internal Memory Organization in 8051. **(08 Marks)**

OR

2 a. With a neat block diagram, explain the architecture of 8051 Microcontroller. **(10 Marks)**

b. Write the circuit diagram for Part – 1. Explain the input, output operations in 8051 using Part – 1. **(10 Marks)**

Module-2

3 a. Explain the different addressing mode of 8051. Give an example for each one of them. **(10 Marks)**

b. Explain the following instructions with examples:
i) SJMP reL ii) DA A iii) CJNE destination , source , reL
iv) SWAP A v) DJNZ Rn , ReL. **(10 Marks)**

OR

4 a. Explain Data transfer instructions with examples. **(10 Marks)**

b. Explain byte and bit level logical AND Operation with example. **(05 Marks)**

c. Write an ALP to verify whether the data present in Accumulator is odd/even if odd store 00H in Ro register. Otherwise store FFH in Ro register. **(05 Marks)**

Module-3

5 a. Write an ALP to find the smallest number of an array of N – 8 bit unsigned numbers. **(08 Marks)**

b. Write an ALP to arrange the Numbers in Ascending order. **(08 Marks)**

c. Write an ALP to rotate the contents of A to the left by one position with carry. **(04 Marks)**

OR

6 a. Write a program to move block of data from Internal data memory to External data memory location. **(10 Marks)**

b. Write a program to find the factorial of a number. **(05 Marks)**

c. Write a program to count the numbers of 1's and 0's in 8 – bit data. **(05 Marks)**

Module-4

7 a. What is the difference between timer and counter? **(02 Marks)**

b. Explain the functions of each bit in the TMOD and TCON register. **(08 Marks)**

c. Write an ALP to generate square wave on Pin P1.5 of 500Hz (approximately) with using timer 0 , mode 1. Assume that crystal frequency of 8051 is 11.0592 MHz. **(10 Marks)**

OR

8 a. Explain Full duplex, Half duplex and Simplex serial data transfer. **(06 Marks)**

b. Write the steps required for programming 8051 to transfer data serially. **(06 Marks)**

c. Write an 8051 C program to transfer the message "YES" serially at 9600 baud , 8 – bit data 1 – stop bit do this continuously. **(08 Marks)**

Module-5

9 a. Explain the function of each bit in the (IE) Interrupt Enable register. **(08 Marks)**

b. Define Interrupt. List the various interrupts of the 8051. **(08 Marks)**

c. Bring out the difference between Interrupt and Pooling. **(04 Marks)**

OR

10 a. A switch is connected to Pin P2.5 and a steeper motor to Port 1. Write a program to monitor the status as of switching and
if Sw = 0 , Stepper motor rotate clockwise,
if Sw = 1 , Stepper motor rotate Anti clockwise continuously. **(10 Marks)**

b. Discuss interfacing of ADC 0804 with 8051 using timing diagram for ADC. **(10 Marks)**

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CBCS SCHEME

USN | 1 | K | S | 1 | 6 | E | C | 0 | 6 | 8 | 17EC563

Fifth Semester B.E. Degree Examination, Dec.2019/Jan.2020
8051 Microcontroller

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write the comparison between Microprocessor and Microcontroller. **(05 Marks)**

b. Define Embedded System and write the characteristics of an Embedded System. **(05 Marks)**

c. Write and explain the Architecture of 8051 Microcontroller and also explain the PSW, RAM memory organization. **(10 Marks)**

OR

2 a. Write and explain the pin diagram of 8051 Microcontroller. **(10 Marks)**

b. Explain the Interfacing of 16K EPROM and 8K RAM to 8051 Microcontroller. **(10 Marks)**

Module-2

3 a. Write and explain the Addressing modes of 8051 Microcontroller with an example. **(10 Marks)**

b. Explain the following instructions with an example:

(i) DJNZ R_n, rel
(ii) MOVC A, @A+DPTR
(iii) RRC A
(iv) PUSH 02
(v) DAA **(10 Marks)**

OR

4 a. Explain Call and Jump Instructions. **(06 Marks)**

b. Explain any four directives. **(04 Marks)**

c. Write and explain an Assembly Language Program to divide the data in RAM location in 38H by data in 15H and store the quotient in 70H and remainder in 71H. **(10 Marks)**

Module-3

5 a. Write and explain an Assembly Language Program to transfer five 8-bit of data from starting memory location 30H to other memory starting at 40H. **(08 Marks)**

b. Write and explain an Assembly Language Program to find largest 8-bit number form the given five 8-bit numbers. **(08 Marks)**

c. Write and explain an Assembly Language Program to toggle all the bits of port 1, with a time delay between toggling. **(04 Marks)**

OR

6 a. Write and explain an Assembly Language Program to read the lower nibble of data by P_0 is to be displayed on LEDS are connected to upper 4-bits of P_1. **(10 Marks)**

b. Write and explain an Assembly Language Program to Add two 32-bit numbers. The numbers are stored from RAM location 40H and 50H respectively. Store the result from RAM location 60H. **(10 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

7 a. Explain TMOD and TCON registers. **(08 Marks)**

b. Write and explain an Assembly language program to toggle $P_{1.5}$ every 1 second. Use Timer1 in mode1. Assume crystal oscillator frequency is 11.0592 MHz. **(08 Marks)**

c. Explain SCON register. **(04 Marks)**

OR

8 a. Write and explain a C program and assembly to generate a square wave of frequency 10 kHz on Pin 1.4. Use timer0 in mode2 with a crystal frequency of 22 MHz. **(10 Marks)**

b. Write and explain a C program and assembly to transfer "VTU" serially with a baud rate of 9600. Assume crystal oscillator frequency is 11.0592 MHz. **(10 Marks)**

Module-5

9 a. Explain IE register. **(04 Marks)**

b. Write and explain a C program and assembly to generate a square wave on $P_{2.4}$ with high of 1 ms and low portion of 2 ms using timer1 in interrupt mode with a crystal oscillator frequency of 11.0592 MHz and also read the value of port0 and display is on port1. **(08 Marks)**

c. Write and explain an assembly language program to do the following:
(i) Reads data from port P_1 and writes it to P_2 continuously.
(ii) Also the data at P_1 is transferred serially.
(iii) The data received serially is displayed at P_0.
Assume 11.0592 MHz crystal frequency 9600 baud rate. **(08 Marks)**

OR

10 a. Write and explain a C program and assembly to interface an ADC 0804 to 8051 Microcontroller and display on P_2. **(10 Marks)**

b. Write and explain a C program and assembly to monitor the status of a switch SW connected to Pin P2.7 and perform the following:
(i) If SW = 0, the stepper motor rotates clockwise.
(ii) If SW = 1, the stepper motor rotates in anticlockwise.
Use the wave-drive 4-step sequence. **(10 Marks)**

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CBCS SCHEME

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15EC563

Fifth Semester B.E. Degree Examination, July/August 2021
8051 Microcontroller

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions.***

1 a. Compare between microprocessor and microcontroller. **(06 Marks)**

b. Explain internal block diagram of 8051. **(10 Marks)**

2 a. Explain internal RAM organization of 8051. **(08 Marks)**

b. Explain External RAM (8K Bytes) interfacing with block diagram and timing. **(08 Marks)**

3 a. Explain any four addressing modes of 8051 with examples. Write a program to copy value of 65H into RAM location 50 to 53H using direct addressing mode without loop. **(10 Marks)**

b. Explain the following instruction with examples: i) XCHD ii) ADDC iii) XRL. **(06 Marks)**

4 a. Explain the following instructions with examples: i) CJNE ii) SETB iii) SJMP iv) JC. **(08 Marks)**

b. Write the instructions to do following:
i) Setting bit1 of internal RAM location 20H.
ii) Reading the content of external RAM location.
iii) Moving a data byte into location of 40H.
iv) Setting carry flag and clearing parity flag without altering other flags. **(04 Marks)**

c. Analyze the following program and write the result after executing each instruction:

```
ORG 00H
MOV R0, #21h
MOV R7, #78h
MOV A, 07h
MOV 21H, A
SETB 0Ah
MOV A, @21h
XRL A, R7
MOVX @R0, A
END
```

(04 Marks)

5 a. Explain working of PUSH and CALL instructions with examples. **(10 Marks)**

b. Develop an assembly language program to count number of 1's in a given byte which is in internal RAM location 50H. Display the result on port P1. **(06 Marks)**

6 a. Develop an assembly language program to find largest in the given N numbers, which are stored in internal RAM location 40H onwards. Store the result in external RAM location 40H, write algorithm. **(10 Marks)**

b. Interface a simple switch and Led to 8051 system and develop the program to read switch status continuously and switch on/off LED accordingly. Draw the block diagram. **(06 Marks)**

7 a. Explain 8051 timer mode-1 programming with steps. **(06 Marks)**

b. Develop an assembly language program to generate square wave of 2000Hz a P1-1 using timer mode-2. Assume crystal frequency of 11.0592MHz. Show the calculations. **(10 Marks)**

8 a. Briefly explain serial communication basics. **(04 Marks)**

b. Draw the Bit pattern of SCON register and explain each bit in it. **(06 Marks)**

c. Develop a program in C/assembly to transmit "VES" serially at 9600 baudrate 1 start and 1 stop bit. Assume crystal frequency of 11.0592MHz. **(06 Marks)**

9 a. Explain 8051 interrupts with their vector address and priority. **(08 Marks)**

b. Develop a 'C' program to generate a square wave of 1kHz using timer interrupt on P1.2. Assume crystal frequency of 12MHz. **(08 Marks)**

10 a. With a block diagram, explain LCD interfacing to 8051. Develop a program in assembly language to display "MCI" on LCD panel. **(10 Marks)**

b. Explain stepper motor interfacing to 8051 with a block diagram and explain how to rotate it 180° clockwise. **(06 Marks)**

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CBCS SCHEME

USN | 1 | K | S | 1 | 6 | E | C | 0 | 6 | 8 |

17EC563

Fifth Semester B.E. Degree Examination, Dec.2019/Jan.2020
8051 Microcontroller

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write the comparison between Microprocessor and Microcontroller. **(05 Marks)**

b. Define Embedded System and write the characteristics of an Embedded System. **(05 Marks)**

c. Write and explain the Architecture of 8051 Microcontroller and also explain the PSW, RAM memory organization. **(10 Marks)**

OR

2 a. Write and explain the pin diagram of 8051 Microcontroller. **(10 Marks)**

b. Explain the Interfacing of 16K EPROM and 8K RAM to 8051 Microcontroller. **(10 Marks)**

Module-2

3 a. Write and explain the Addressing modes of 8051 Microcontroller with an example. **(10 Marks)**

b. Explain the following instructions with an example:
(i) DJNZ R_n, rel
(ii) MOVC A, @A+DPTR
(iii) RRC A
(iv) PUSH 02
(v) DAA **(10 Marks)**

OR

4 a. Explain Call and Jump Instructions. **(06 Marks)**

b. Explain any four directives. **(04 Marks)**

c. Write and explain an Assembly Language Program to divide the data in RAM location in 38H by data in 15H and store the quotient in 70H and remainder in 71H. **(10 Marks)**

Module-3

5 a. Write and explain an Assembly Language Program to transfer five 8-bit of data from starting memory location 30H to other memory starting at 40H. **(08 Marks)**

b. Write and explain an Assembly Language Program to find largest 8-bit number form the given five 8-bit numbers. **(08 Marks)**

c. Write and explain an Assembly Language Program to toggle all the bits of port 1, with a time delay between toggling. **(04 Marks)**

OR

6 a. Write and explain an Assembly Language Program to read the lower nibble of data by P_0 is to be displayed on LEDS are connected to upper 4-bits of P_1. **(10 Marks)**

b. Write and explain an Assembly Language Program to Add two 32-bit numbers. The numbers are stored from RAM location 40H and 50H respectively. Store the result from RAM location 60H. **(10 Marks)**

Module-4

7 a. Explain TMOD and TCON registers. (08 Marks)
b. Write and explain an Assembly language program to toggle $P_{1.5}$ every 1 second. Use Timer1 in mode1. Assume crystal oscillator frequency is 11.0592 MHz. (08 Marks)
c. Explain SCON register. (04 Marks)

OR

8 a. Write and explain a C program and assembly to generate a square wave of frequency 10 kHz on Pin 1.4. Use timer0 in mode2 with a crystal frequency of 22 MHz. (10 Marks)
b. Write and explain a C program and assembly to transfer "VTU" serially with a baud rate of 9600. Assume crystal oscillator frequency is 11.0592 MHz. (10 Marks)

Module-5

9 a. Explain IE register. (04 Marks)
b. Write and explain a C program and assembly to generate a square wave on $P_{2.4}$ with high of 1 ms and low portion of 2 ms using timer1 in interrupt mode with a crystal oscillator frequency of 11.0592 MHz and also read the value of port0 and display is on port1. (08 Marks)
c. Write and explain an assembly language program to do the following:
(i) Reads data from port P_1 and writes it to P_2 continuously.
(ii) Also the data at P_1 is transferred serially.
(iii) The data received serially is displayed at P_0.
Assume 11.0592 MHz crystal frequency 9600 baud rate. (08 Marks)

OR

10 a. Write and explain a C program and assembly to interface an ADC 0804 to 8051 Microcontroller and display on P_2. (10 Marks)
b. Write and explain a C program and assembly to monitor the status of a switch SW connected to Pin P2.7 and perform the following:
(i) If SW = 0, the stepper motor rotates clockwise.
(ii) If SW = 1, the stepper motor rotates in anticlockwise.
Use the wave-drive 4-step sequence. (10 Marks)

* * * * *

R. S. Institute of Technology, Bangalore -109

Department of Electronics and Communication Engineering

4th sem Course End Survey 2020-21

Course : Microcontroller -2021 Course Code :18EC46

Q1.How is your understanding on Architecture of 8051 and interfacing of 8051 to external memory?
Q2.Rate yourself on understanding of instruction set of 8051?
Q3.How well are you able to write 8051 assembly level programs using 8051 instruction set?
Q4.How well are you able to write assembly language program to configure Microcontroller as timers, counters and serial port to send & receive data serially?
Q5.How is your knowledge on 8051 interrupts and interfacing applications?

Sl No	Date	Name of the Student	USN	semester & section	Faculty Name	Q1	Q2	Q3	Q4	Q5
1	8/17/2021 10:45:54	Sneha n	1KS18EC089	4th B section	Mr. S Christo Jain	3	3	3	3	3
2	8/16/2021 8:55:33	Abhilash A S	1KS19EC001	4th A	Mr. Sunil Kumar G R	2	2	2	2	2
3	8/13/2021 21:53:42	Abhishek C	1KS19EC002	4 A	Mr. Sunil Kumar G R	2	2	2	2	2
4	8/13/2021 21:52:42	Aishwarya basavaraja kembavi	1KS19EC003	4 'A'	Mr. Sunil Kumar G R	3	3	3	2	3
5	8/17/2021 12:43:02	Aishwarya MG	1KS19EC004	4th sem A sec	Mr. Sunil Kumar G R	3	3	3	3	3
6	8/13/2021 15:20:50	Akshitha	1KS19EC006	4th, A sec	Mr. Sunil Kumar G R	3	3	3	3	3
7	8/13/2021 16:43:38	AMRUTA	1KS19EC007	4 sem - A sec	Mr. Sunil Kumar G R	3	3	3	3	3
8	8/13/2021 15:47:31	Amulya	1KS19EC008	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
9	8/13/2021 15:32:44	Anitha.S	1KS19EC009	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
10	8/17/2021 11:19:44	Anjali Y J	1KS19EC010	4th sem A sec	Mr. Sunil Kumar G R	2	2	2	2	2
11	8/17/2021 11:00:47	Archana Yadav M	1KS19EC011	4 th sem A sec	Mr. Sunil Kumar G R	3	3	3	3	3
12	8/17/2021 10:44:55	Ashritha.R	1KS19EC012	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
13	8/18/2021 11:36:55	Bhavana S	1KS19EC014	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
14	8/17/2021 20:24:24	Chaitra p	1KS19EC015	4th A	Mr. Sunil Kumar G R	3	3	3	3	3
15	8/13/2021 19:37:52	Chandana	1KS19EC017	4sem A sec	Mr. Sunil Kumar G R	3	3	3	3	3
16	8/17/2021 12:59:38	Chennreddy Rajasekhar	1KS19EC018	4A	Mr. Sunil Kumar G R	3	2	3	3	1
17	8/13/2021 15:44:16	Chiranthana Yogananda.K	1KS19EC019	4th sem A section	Mr. Sunil Kumar G R	2	2	2	2	2
18	8/17/2021 16:00:04	D Nayan	1KS19EC020	4th sem A sec	Mr. Sunil Kumar G R	3	3	3	3	3
19	8/13/2021 15:37:44	Danesh Raju v	1KS19EC021	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
20	8/13/2021 15:15:49	Davino Joseph	1KS19EC022	4 a	Mr. Sunil Kumar G R	3	3	3	3	3
21	8/13/2021 23:42:15	DHEEMANTH KN	1KS19EC024	IV 'A'	Mr. Sunil Kumar G R	3	3	3	3	3
22	8/13/2021 15:16:13	Disha Shivani	1KS19EC025	4 A	Mr. Sunil Kumar G R	2	2	2	2	2
23	8/17/2021 13:49:04	Gayathri .P.K	1KS19EC027	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
24	8/17/2021 10:52:44	Gayathri R Warrier	1KS19EC028	4 sem A ece	Mr. Sunil Kumar G R	3	3	3	3	3
25	8/17/2021 10:52:57	GONUGUNTLA SAI SIDDARTH	1KS19EC029	4&A	Mr. Sunil Kumar G R	3	3	3	3	3
26	8/14/2021 11:11:29	Gowri	1KS19EC030	4,A	Mr. Sunil Kumar G R	3	3	3	2	3
27	8/17/2021 10:44:37	B.Y Harshitha	1KS19EC032	4th sem ,Asec	Mr. Sunil Kumar G R	2	2	2	1	2
28	8/17/2021 12:31:17	Hemanth	1KS19EC033	4th A sec	Mr. Sunil Kumar G R	3	3	3	3	3
29	8/13/2021 15:46:14	Jagruti Pai	1KS19EC035	IV SEM A SEC	Mr. Sunil Kumar G R	3	2	2	3	3

30	8/13/2021 15:19:24	Manogna K M	1KS19EC037	4th sem,A-section	Mr. Sunil Kumar G R	3	3	3	3	3
31	8/13/2021 20:40:39	Karthik.K	1KS19EC038	4th sem A	Mr. Sunil Kumar G R	3	3	3	3	3
32	8/17/2021 11:47:43	Kashyap p	1KS19EC039	4 A	Mr. Sunil Kumar G R	3	2	2	3	2
33	8/13/2021 16:59:18	Krupa A	1KS19EC040	4th A	Mr. Sunil Kumar G R	3	3	3	3	3
34	8/13/2021 15:41:03	LAKSHMAN KUMARA B	1KS19EC042	4th sem & A section	Mr. Sunil Kumar G R	3	3	3	3	3
35	8/17/2021 20:22:32	Likitha H	1KS19EC043	4A	Mr. Sunil Kumar G R	3	3	3	3	3
36	8/13/2021 15:22:22	M.Lokeshwari	1KS19EC044	4 sem and A sec	Mr. Sunil Kumar G R	3	3	3	3	3
37	8/13/2021 15:21:47	Manu N kandra	1KS19EC045	4th sem A sec	Mr. Sunil Kumar G R	3	3	3	3	3
38	8/13/2021 21:54:00	Meghana H P	1KS19EC046	4th & A	Mr. Sunil Kumar G R	3	3	3	3	3
39	8/17/2021 10:55:12	MOHAMMAD RAKHEEB M R	1KS19EC047	4th A sem	Mr. Sunil Kumar G R	2	2	2	2	2
40	8/17/2021 10:44:36	Monika v arya	1KS19EC049	4th A	Mr. Sunil Kumar G R	3	3	3	3	3
41	8/17/2021 10:48:11	Monisha B K	1KS19EC050	4sem A section	Mr. Sunil Kumar G R	3	3	3	3	3
42	8/13/2021 19:16:00	N.ANILA	1KS19EC051	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
43	8/17/2021 10:44:55	Nidhi. S	1KS19EC052	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
44	8/17/2021 10:58:34	Nisarga k	1KS19EC053	4 a	Mr. Sunil Kumar G R	3	3	3	3	3
45	8/17/2021 12:33:02	NITHIN D	1KS19EC054	4 A	Mr. Sunil Kumar G R	3	3	3	3	3
46	8/13/2021 15:45:17	Pavan Kumar G R	1KS19EC055	4th Sem A Section	Mr. Sunil Kumar G R	3	3	2	3	3
47	8/13/2021 15:17:31	Pokuri Mounika	1KS19EC056	4,A	Mr. Sunil Kumar G R	2	3	1	2	2
48	8/13/2021 15:13:03	PRASHANTH SK	1KS19EC061	4 & A	Mr. Sunil Kumar G R	3	3	3	3	3
49	8/13/2021 16:21:30	Praveen Kumar. N	1KS19EC062	4th sem & Asec	Mr. Sunil Kumar G R	2	2	2	2	2
50	8/13/2021 23:53:54	PREETHAM GH	1KS19EC063	4 th sem, A section	Mr. Sunil Kumar G R	3	2	2	2	2
51	8/17/2021 10:50:46	Priyanka K	1KS19EC064	4th sem A sec	Mr. Sunil Kumar G R	3	3	3	3	3
52	8/13/2021 15:39:10	Radhakrishna L	1KS19EC065	4 A	Mr. Sunil Kumar G R	3	3	2	2	2
53	8/13/2021 15:14:26	Rajalakshmi S	1KS19EC066	4-A	Mr. Sunil Kumar G R	2	2	2	2	2
54	8/13/2021 15:15:53	Ramya sree.R	1KS19EC067	4th sem B sec	Mr. S Christo Jain	2	2	2	2	2
55	8/17/2021 11:19:36	RANGASWAMY U	1KS19EC068	IV SEM B SECTION	Mr. S Christo Jain	3	3	3	3	3
56	8/17/2021 10:47:37	Rohan K R	1KS19EC069	4th semester B secti	Mr. S Christo Jain	3	3	3	3	3
57	8/14/2021 8:43:24	S.K Bharatesh	1KS19EC070	4th sem B section	Mr. S Christo Jain	3	3	3	3	3
58	8/17/2021 11:30:28	Sabarish IJ	1KS19EC071	4th B	Mr. S Christo Jain	3	3	3	3	2
59	8/13/2021 15:34:41	Sahana.KS	1KS19EC072	4 B	Mr. S Christo Jain	3	3	3	2	2
60	8/13/2021 15:22:08	Sahana.S	1KS19EC073	4th sem B sec	Mr. S Christo Jain	3	3	3	3	3
61	8/13/2021 15:34:47	Sai priya ts	1KS19EC074	4th n B sec	Mr. S Christo Jain	3	3	3	3	3
62	8/17/2021 10:46:27	Samiksha S	1KS19EC075	Fourth sem b section	Mr. S Christo Jain	3	3	3	3	3
63	8/17/2021 10:45:05	Santosh Hegde	1KS19EC076	4th Sem B	Mr. S Christo Jain	3	3	3	3	3
64	8/13/2021 15:14:08	SATHVIK U.M	1KS19EC077	4th B	Mr. S Christo Jain	3	3	3	3	3
65	8/17/2021 11:06:40	Shamitha	1KS19EC078	4th sem & b sec	Mr. S Christo Jain	3	3	3	3	3
66	8/13/2021 16:02:36	SHASHANK KASHYAP HR	1KS19EC079	4B	Mr. S Christo Jain	2	2	2	2	2
67	8/13/2021 16:01:28	Shreyams D.K	1KS19EC081	4 and B sec	Mr. S Christo Jain	2	2	2	2	2
68	8/13/2021 15:44:07	Shreyas B Aradhya	1KS19EC082	4th sem B section	Mr. S Christo Jain	3	2	2	3	3
69	8/17/2021 10:59:23	Shreyas Gowda	1KS19EC083	IV B	Mr. S Christo Jain	3	3	3		3
70	8/17/2021 10:48:20	Shreyas V Bharadwaj	1KS19EC084	4 & B	Mr. S Christo Jain	3	3	2	3	3
71	8/13/2021 15:19:20	Shubham Kumar Singh A	1KS19EC085	4TH B	Mr. S Christo Jain	2	2	2	2	2
72	8/17/2021 11:11:25	SINCHANA MN	1KS19EC086	4th seen & b sec	Mr. S Christo Jain	3	3	3	3	3

73	8/17/2021 10:45:34	Srinivas S	1KS19EC087	4 B	Mr. S Christo Jain	2	2	2	2	1
74	8/17/2021 11:00:10	Srinivasan	1KS19EC088	4 B	Mr. S Christo Jain	3	3	3	3	3
75	8/17/2021 10:58:21	Suhas M	1KS19EC090	4th sem B Sec	Mr. S Christo Jain	3	3	3	3	3
76	8/13/2021 15:57:51	SUMUKHA VASISHTA MR	1KS19EC092	4TH SEM B SEC	Mr. S Christo Jain	2	2	2	2	2
77	8/17/2021 11:11:36	Sushmitha	1KS19EC093	4th B	Mr. S Christo Jain	3	3	3	3	3
78	8/13/2021 15:13:20	1ks19ec094	1KS19EC094	4 th b	Mr. S Christo Jain	2	2	2	2	2
79	8/17/2021 14:14:56	SWATHI.U	1KS19EC095	4th sem 'B'	Mr. S Christo Jain	3	2	2	2	2
80	8/13/2021 20:37:32	T N L RUTHVIK	1KS19EC096	4B	Mr. S Christo Jain	3	3	3	3	3
81	8/13/2021 15:35:08	Tejashwini pv	1KS19EC097	4th sem bsec	Mr. S Christo Jain	3	3	3	2	3
82	8/17/2021 11:34:51	Theerthana s r	1KS19EC098	4th sem B sec	Mr. S Christo Jain	3	3	3	3	3
83	8/14/2021 5:50:03	Theerthana s r	1KS19EC098	4th sem Bsec	Mr. S Christo Jain	3	3	3	3	3
84	8/13/2021 15:16:36	Tushar R Vasishta	1KS19EC099	4 B	Mr. S Christo Jain	2	2	2	2	2
85	8/13/2021 21:07:05	Vandana.G	1KS19EC101	4th sem B sec	Mr. S Christo Jain	3	3	3	3	3
86	8/17/2021 10:52:36	Vandana S	1KS19EC102	4 b	Mr. S Christo Jain	3	3	3	2	3
87	8/17/2021 11:37:59	Vignesh muthaiah R	1KS19EC103	4/B	Mr. S Christo Jain	3	3	3	3	3
88	8/13/2021 18:16:15	Vikas.S	1KS19EC104	4th sem B sec	Mr. S Christo Jain	3	2	2	2	2
89	8/13/2021 18:23:30	VINUTH S REDDY	1KS19EC105	4 th sem B	Mr. S Christo Jain	3	2	3	2	3
90	8/13/2021 18:12:31	Vishal Sanjay Raju	1KS19EC106	4 sem B section	Mr. S Christo Jain	3	3	3	3	3
91	8/17/2021 10:55:31	Vishnuraata Yadunandan	1KS19EC107	4th B	Mr. S Christo Jain	2	2	2	2	2
92	8/13/2021 15:31:14	yashaswini.N	1KS19EC108	4th sem B sec	Mr. S Christo Jain	3	3	3	3	3
93	8/13/2021 17:50:40	Vaishnavi k	1KS19EC109	4th sem & B sec	Mr. S Christo Jain	2	2	2	2	2
94	8/17/2021 12:34:12	Chaitra C	1KS19ET002	4th sem & B sec	Mr. S Christo Jain	3	3	3	3	3
95	8/17/2021 10:54:43	Litchitha Gowda	1KS19ET003	4B	Mr. S Christo Jain	2	2	2	2	2
96	8/17/2021 12:36:07	Nelbin	1KS19ET006	4 B	Mr. S Christo Jain	2	2	2	2	2
97	8/13/2021 16:16:31	Niranjan S Rao	1KS19ET007	4th sem B sec	Mr. S Christo Jain	3	3	2	2	3
98	8/17/2021 10:46:45	Rishi Kumar s	1KS19ET008	4th sem Bsec	Mr. S Christo Jain	1	1	1	1	1
99	8/17/2021 10:45:49	ROHIT KUMAR	1KS19ET009	4th B	Mr. S Christo Jain	3	3	3	3	3
100	8/13/2021 15:15:34	Shreyas c r	1KS19ET010	4th , B sec	Mr. S Christo Jain	2	3	3	3	3
101	8/17/2021 10:53:33	Shwetha k	1KS19ET011	4th sem B	Mr. S Christo Jain	2	3	2	2	3
102	8/17/2021 12:31:06	Ranjana p	1KS20EC401	4th B sec	Mr. S Christo Jain	2	2	2	2	2
					No.of 1s	**1**	**1**	**2**	**2**	**3**
					Total	**102**	**102**	**102**	**101**	**102**
					percentage	**99**	**99**	**98**	**98**	**97**
					Average	**98**				

K.S. INSTITUTE OF TECHNOLOGY, BANGALORE
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

YEAR / SEMESTER	**II / IV**
COURSE TITLE	**Microcontroller**
COURSE CODE	**18EC46**
ACADEMIC YEAR	**2020-2021**
BATCH	**2019 - 2023**

	Significance
Le	60% and above students should have scored >= 60% of
Le	55% to 59% of students should have scored >= 60% of
Le	50% to 54% of students should have scored >= 60% of

For Direct attainment , 50% of CIE and 50% of SEE marks are con
For indirect attainment, Course end survey is considered.
CO attainment is 90%of direct attainment + 10% of Indirect attta
PO attainment = CO-PO mapping strength/3 * CO attainment .

Sl. NO.	USN	NAME	IA1							Assignment 1							IA2										Assignment 2										IA3							Assignment 3							EXTERNAL MARKS			
			IA1	CO1	score		Target 60 %	CO2	score	Target 60 %	A1	CO1	score	Target 60 %	CO2	score	Target 60%	IA2	CO2	score	Target 60%	CO3	score	Target 60 %	CO4	score	Target 60 %	A2	CO2	score	Target 60%	CO3	score	Target 60%	CO4	score	Target 60%	IA3	CO4	score	Target 60%	CO5	score	Target 60 %	A3	CO4	score	Target 60 %	CO5	score	Target 60 %	SEE	SEE	score	Target 60 %
	Maximum Marks		30	18			12				10	6			4			30	6			18			6			10	2			6			2			30	12			18			10	6			4			50	60		
1	1KS19EC001	ABHILASH A S	24	14	3	Y	10	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	28	11	3	Y	17	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
2	1KS19EC002	ABHISHEK CHANDRESH	23	14	3	Y	9	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	10	3	Y	17	3	Y	10	6	3	Y	4	3	Y	18	22	0	N
3	1KS19EC003	AISHWARYA BASAVARAJ	23	14	3	Y	9	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	29	11	3	Y	18	3	Y	10	6	3	Y	4	3	Y	31	37	1	N
4	1KS19EC004	AISHWARYA M G	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	25	12	3	Y	13	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
5	1KS19EC005	AKSHAY KUMAR D	23	13	3	Y	10	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	11	3	Y	13	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
6	1KS19EC006	AKSHITHA	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	29	11	3	Y	18	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
7	1KS19EC007	AMRUTA	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	22	6	3	Y	12	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	28	11	3	Y	17	3	Y	10	6	3	Y	4	3	Y	25	30	0	N
8	1KS19EC008	AMULYA R	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	27	6	3	Y	17	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	23	10	3	Y	13	3	Y	10	6	3	Y	4	3	Y	35	42	2	N
9	1KS19EC009	ANITHA S	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	26	6	3	Y	16	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	29	12	3	Y	17	3	Y	10	6	3	Y	4	3	Y	31	37	1	N
10	1KS19EC010	ANJALI Y J	27	16	3	Y	11	3	Y	10	6	3	Y	4	3	Y	28	6	3	Y	18	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	27	32	0	N
11	1KS19EC011	ARCHANA YADAV M	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	10	3	Y	14	3	Y	10	6	3	Y	4	3	Y	31	37	1	N
12	1KS19EC012	ASHRITHA R	22	13	3	Y	9	3	Y	10	6	3	Y	4	3	Y	28	6	3	Y	18	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	25	9	3	Y	16	3	Y	10	6	3	Y	4	3	Y	22	26	0	N
13	1KS19EC014	BHAVANA S	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	11	3	Y	16	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
14	1KS19EC015	CHAITRA P	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	27	6	3	Y	17	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	11	3	Y	16	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
15	1KS19EC016	CHANDAN RAJ Y	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	28	6	3	Y	18	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	25	8	3	Y	17	3	Y	10	6	3	Y	4	3	Y	28	34	0	N
16	1KS19EC017	CHANDANA.L	22	12	3	Y	10	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	9	3	Y	17	3	Y	10	6	3	Y	4	3	Y	26	31	0	N
17	1KS19EC018	CHENNREDDY RAJASEKHAR	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	22	6	3	Y	12	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	11	3	Y	13	3	Y	10	6	3	Y	4	3	Y	34	41	2	N
18	1KS19EC019	CHIRANTHANA YOGANANDA K	22	13	3	Y	9	3	Y	10	6	3	Y	4	3	Y	25	6	3	Y	15	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	11	3	Y	13	3	Y	10	6	3	Y	4	3	Y	21	25	0	N
19	1KS19EC020	D NAYAN	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	11	3	Y	16	3	Y	10	6	3	Y	4	3	Y	25	30	0	N
20	1KS19EC021	DANESH RAJU V	23	13	3	Y	10	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
21	1KS19EC022	DAVINO JOSEPH	23	13	3	Y	10	3	Y	10	6	3	Y	4	3	Y	28	6	3	Y	18	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	11	3	Y	16	3	Y	10	6	3	Y	4	3	Y	29	35	0	N
22	1KS19EC023	DHANYA SUKANTH B K	23	13	3	Y	10	3	Y	10	6	3	Y	4	3	Y	26	6	3	Y	17	3	Y	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	26	9	3	Y	17	3	Y	10	6	3	Y	4	3	Y	31	37	1	N
23	1KS19EC024	DHEEMANTH K N	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	11	3	Y	13	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
24	1KS19EC025	DISHA SHIVANI	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	10	3	Y	14	3	Y	10	6	3	Y	4	3	Y	37	44	3	Y
25	1KS19EC027	GAYATHRI P K	23	13	3	Y	10	3	Y	10	6	3	Y	4	3	Y	26	6	3	Y	16	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	9	3	Y	17	3	Y	10	6	3	Y	4	3	Y	28	34	0	N
26	1KS19EC028	GAYATHRI R WARRIER	26	16	3	Y	10	3	Y	10	6	3	Y	4	3	Y	25	6	3	Y	15	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	10	3	Y	17	3	Y	10	6	3	Y	4	3	Y	36	43	3	Y
27	1KS19EC029	GONUGUNTLA SAI SIDDARTHA	23	13	3	Y	10	3	Y	10	6	3	Y	4	3	Y	22	6	3	Y	12	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	9	3	Y	15	3	Y	10	6	3	Y	4	3	Y	20	24	0	N
28	1KS19EC030	GOWRI S NADIGER	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	29	11	3	Y	18	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
29	1KS19EC031	HARSHA R	20	10	2	N	10	3	Y	10	6	3	Y	4	3	Y	22	6	3	Y	12	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	25	10	3	Y	15	3	Y	10	6	3	Y	4	3	Y	22	26	0	N
30	1KS19EC032	HARSHITHA B Y	23	13	3	Y	10	3	Y	10	6	3	Y	4	3	Y	21	6	3	Y	11	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	12	3	Y	12	3	Y	10	6	3	Y	4	3	Y	30	36	1	N

31	1KS19EC033	HEMANTH.R.PATIL	23	13	3	Y	10	3	Y	10	6	3	Y	4	3	Y	21	4	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	12	3	Y	15	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
32	1KS19EC035	JAGRUTI PAI	26	15	3	Y	11	3	Y	10	6	3	Y	4	3	Y	29	6	3	Y	18	3	Y	5	3	Y	10	2	3	Y	6	3	Y	2	3	Y	28	11	3	Y	17	3	Y	10	6	3	Y	4	3	Y	40	48	3	Y
33	1KS19EC036	JAYANTH M B	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	5	3	Y	15	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	9	3	Y	17	3	Y	10	6	3	Y	4	3	Y	20	24	0	N
34	1KS19EC037	KAMMA MANUBOLU MANOGNA	20	11	3	Y	9	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	29	12	3	Y	17	3	Y	10	6	3	Y	4	3	Y	23	28	0	N
35	1KS19EC038	KARTHIK K	23	12	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	12	3	Y	12	3	Y	10	6	3	Y	4	3	Y	27	32	0	N
36	1KS19EC039	KASHYAP.P	22	14	3	Y	8	3	Y	10	6	3	Y	4	3	Y	28	6	3	Y	18	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	11	3	Y	15	3	Y	10	6	3	Y	4	3	Y	23	28	0	N
37	1KS19EC040	KRUPA.A	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	20	6	3	Y	10	2	N	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	25	11	3	Y	14	3	Y	10	6	3	Y	4	3	Y	34	41	2	N
38	1KS19EC041	KRUTHI K S	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	26	6	3	Y	16	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	12	3	Y	14	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
39	1KS19EC042	LAKSHMAN KUMARA B	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	22	6	3	Y	12	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	11	3	Y	16	3	Y	10	6	3	Y	4	3	Y	23	28	0	N
40	1KS19EC043	LIKITHA.H	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	28	6	3	Y	18	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	28	11	3	Y	17	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
41	1KS19EC044	M LOKESHWARI	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	29	12	3	Y	17	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
42	1KS19EC045	MANU N KANDRA	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	22	6	3	Y	12	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	29	11	3	Y	18	3	Y	10	6	3	Y	4	3	Y	31	37	1	N
43	1KS19EC046	MEGHANA H P	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	12	3	Y	12	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
44	1KS19EC047	MOHAMMAD RAKHEEB M R	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	26	6	3	Y	16	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	22	9	3	Y	13	3	Y	10	6	3	Y	4	3	Y	22	26	0	N
45	1KS19EC048	MOHITH KUMAR G	23	15	3	Y	8	3	Y	10	6	3	Y	4	3	Y	27	5	3	Y	17	3	Y	5	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	12	3	Y	12	3	Y	10	6	3	Y	4	3	Y	19	23	0	N
46	1KS19EC049	MONIKA V ARYA	24	13	3	Y	11	3	Y	10	6	3	Y	4	3	Y	26	6	3	Y	16	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	25	12	3	Y	13	3	Y	10	6	3	Y	4	3	Y	20	24	0	N
47	1KS19EC050	MONISHA.B.K	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	26	6	3	Y	16	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	12	3	Y	14	3	Y	10	6	3	Y	4	3	Y	31	37	1	N
48	1KS19EC051	N ANILA	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	28	6	3	Y	18	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	12	3	Y	14	3	Y	10	6	3	Y	4	3	Y	35	42	2	N
49	1KS19EC052	NIDHI S	23	12	3	Y	11	3	Y	10	6	3	Y	4	3	Y	20	6	3	Y	10	2	N	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	27	9	3	Y	18	3	Y	10	6	3	Y	4	3	Y	16	19	0	N
50	1KS19EC053	NISARGA K	22	14	3	Y	8	3	Y	10	6	3	Y	4	3	Y	19	6	3	Y	9	1	N	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	10	3	Y	14	3	Y	10	6	3	Y	4	3	Y	28	34	0	N
51	1KS19EC054	NITHIN D	24	14	3	Y	10	3	Y	10	6	3	Y	4	3	Y	27	6	3	Y	17	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	23	10	3	Y	13	3	Y	10	6	3	Y	4	3	Y	24	29	0	N
52	1KS19EC055	PAVAN KUMAR G R	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	12	3	Y	12	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
53	1KS19EC056	POKURI MOUNIKA	19	14	3	Y	5	0	N	10	6	3	Y	4	3	Y	23	6	3	Y	13	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	10	3	Y	16	3	Y	10	6	3	Y	4	3	Y	27	32	0	N
54	1KS19EC057	POOJA S P	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	12	3	Y	14	3	Y	10	6	3	Y	4	3	Y	25	30	0	N
55	1KS19EC058	PRADEEP GADED	24	14	3	Y	10	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	23	11	3	Y	12	3	Y	10	6	3	Y	4	3	Y	21	25	0	N
56	1KS19EC059	PRAKASH CHEGORE	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	11	3	Y	13	3	Y	10	6	3	Y	4	3	Y	21	25	0	N
57	1KS19EC061	PRASHANTH.S.K	26	14	3	Y	12	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	25	12	3	Y	13	3	Y	10	6	3	Y	4	3	Y	35	42	2	N
58	1KS19EC062	PRAVEEN KUMAR N	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	23	11	3	Y	12	3	Y	10	6	3	Y	4	3	Y	20	24	0	N
59	1KS19EC063	PREETHAM G H	23	12	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	24	11	3	Y	13	3	Y	10	6	3	Y	4	3	Y	29	35	0	N
60	1KS19EC064	PRIYANKA K	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	27	6	3	Y	17	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	26	12	3	Y	14	3	Y	10	6	3	Y	4	3	Y	21	25	0	N
61	1KS19EC065	RADHA KRISHNA L	25	14	3	Y	11	3	Y	10	6	3	Y	4	3	Y	24	6	3	Y	14	3	Y	4	3	Y	10	2	3	Y	6	3	Y	2	3	Y	25	11	3	Y	14	3	Y	10	6	3	Y	4	3	Y	23	28	0	N
62	1KS19EC066	RAJALAKSHMI S	27	16	3	Y	11	3	Y	10	6	3	Y	4	3	Y	27	6	3	Y	18	3	Y	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	22	9	3	Y	13	3	Y	10	6	3	Y	4	3	Y	32	38	1	N
63	1KS19EC067	RAMYASREE R	28	18	3	Y	10	3	Y	10	6	3	Y	4	3	Y	27	6	3	Y	15	3	Y	6	3	Y	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	24	29	0	N
64	1KS19EC068	RANGASWAMY.U	20	11	3	Y	9	3	Y	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	32	38	1	N
65	1KS19EC069	ROHAN K R	22	13	3	Y	9	3	Y	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
66	1KS19EC070	S K BHARATESH	29	18	3	Y	11	3	Y	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	36	43	3	Y
67	1KS19EC071	SABARISH I J	19	10	2	N	9	3	Y	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	22	26	0	N
68	1KS19EC072	SAHANA K S	25	16	3	Y	9	3	Y	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
69	1KS19EC073	SAHANA S	26	16	3	Y	10	3	Y	10	6	3	Y	4	3	Y	25	6	3	Y	16	3	Y	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	34	41	2	N
70	1KS19EC074	SAI PRIYA T S	28	17	3	Y	11	3	Y	10	6	3	Y	4	3	Y	14	5	3	Y	6	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	29	12	3	Y	17	3	Y	10	6	3	Y	4	3	Y	26	31	0	N
71	1KS19EC075	SAMIKSHA S	16	7	0	N	9	3	Y	10	6	3	Y	4	3	Y	14	5	3	Y	3	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	17	20	0	N
72	1KS19EC076	SANTOSH HEGDE	23	14	3	Y	9	3	Y	10	6	3	Y	4	3	Y	16	5	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	31	37	1	N
73	1KS19EC077	SATHVIK U M	18	9	1	N	9	3	Y	10	6	3	Y	4	3	Y	11	5	3	Y	3	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	21	25	0	N
74	1KS19EC078	SHAMITHA BIJOOR	21	15	3	Y	6	1	N	10	6	3	Y	4	3	Y	22	5	3	Y	14	3	Y	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	34	41	2	N

75	1KS19EC079	SHASHANK KASHYAP.H.R	26	16	3	Y	10	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	28	34	0	N
76	1KS19EC081	SHREYAMS D K	22	15	3	Y	7	2	N	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
77	1KS19EC082	SHREYAS B ARADHYA	18	11	3	Y	7	2	N	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	28	34	0	N
78	1KS19EC083	SHREYAS GOWDA	25	15	3	Y	10	3	Y	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	24	29	0	N
79	1KS19EC084	SHREYAS V BHARADWAJ	28	18	3	Y	10	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	35	42	2	N
80	1KS19EC085	SHUBHAM KUMAR SINGH	28	18	3	Y	10	3	Y	10	6	3	Y	4	3	Y	16	4	3	Y	9	1	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	27	32	0	N
81	1KS19EC086	SINCHANA M N	21	13	3	Y	8	3	Y	10	6	3	Y	4	3	Y	21	4	3	Y	14	3	Y	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	33	40	2	N
82	1KS19EC087	SRINIVAS S	28	18	3	Y	10	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	29	35	0	N
83	1KS19EC088	SRINIVASAN M	24	16	3	Y	8	3	Y	10	6	3	Y	4	3	Y	24	4	3	Y	14	3	Y	6	3	Y	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	38	46	3	Y
84	1KS19EC089	SRIRAM	21	12	3	Y	9	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	26	31	0	N
85	1KS19EC090	SUHAS.M	27	17	3	Y	10	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	29	35	0	N
86	1KS19EC092	SUMUKHA VASISHTA M R	26	16	3	Y	10	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
87	1KS19EC093	SUSHMITHA S	24	16	3	Y	8	3	Y	10	6	3	Y	4	3	Y	21	4	3	Y	14	3	Y	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	38	46	3	Y
88	1KS19EC094	SWAGATH AITHAL P G	27	17	3	Y	10	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
89	1KS19EC095	SWATHI U	21	14	3	Y	7	2	N	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	27	32	0	N
90	1KS19EC096	T N L RUTHVIK	24	16	3	Y	8	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
91	1KS19EC097	TEJASHWINI P V	24	16	3	Y	8	3	Y	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	26	31	0	N
92	1KS19EC098	THEERTHANA S R	28	18	3	Y	10	3	Y	10	6	3	Y	4	3	Y	21	4	3	Y	14	3	Y	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	31	37	1	N
93	1KS19EC099	TUSHAR R VASISHTA	23	14	3	Y	9	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	21	25	0	N
94	1KS19EC100	VAISHNAVI K	23	15	3	Y	8	3	Y	10	6	3	Y	4	3	Y	17	4	3	Y	10	2	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	22	26	0	N
95	1KS19EC101	VANDANA G	25	16	3	Y	9	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	36	43	3	Y
96	1KS19EC102	VANDANA S	26	16	3	Y	10	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	25	30	0	N
97	1KS19EC103	VIGNESH MUTHAIAH R	26	16	3	Y	10	3	Y	10	6	3	Y	4	3	Y	28	5	3	Y	18	3	Y	5	3	Y	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	30	36	1	N
98	1KS19EC104	VIKAS S	28	18	3	Y	10	3	Y	10	6	3	Y	4	3	Y	14	4	3	Y	7	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	18	22	0	N
99	1KS19EC105	VINUTH S REDDY	23	14	3	Y	9	3	Y	10	6	3	Y	4	3	Y	15	4	3	Y	8	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	11	13	0	N
100	1KS19EC106	VISHAL SANJAY RAJU	26	16	3	Y	10	3	Y	10	6	3	Y	4	3	Y	12	4	3	Y	2	0	N	6	3	Y	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	27	32	0	N
101	1KS19EC107	VISHNU RAATA YADUNANDAN	20	12	3	Y	8	3	Y	10	6	3	Y	4	3	Y	11	4	3	Y	4	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	28	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	32	38	1	N
102	1KS19EC108	YASHASWINI N	25	15	3	Y	10	3	Y	10	6	3	Y	4	3	Y	14	4	3	Y	7	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	30	12	3	Y	18	3	Y	10	6	3	Y	4	3	Y	29	35	0	N
103	1KS20EC400	MADALA VIVEK KUMAR	16	13	3	Y	6	1	N	10	6	3	Y	4	3	Y	16	4	3	Y	7	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	27	11	3	Y	14	3	Y	10	6	3	Y	4	3	Y	15	18	0	N
104	1KS20EC401	RANJANA	19	16	3	Y	8	3	Y	10	6	3	Y	4	3	Y	16	4	3	Y	6	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	25	9	3	Y	13	3	Y	10	6	3	Y	4	3	Y	19	23	0	N
105	1KS20EC402	SINDHU	24	17	3	Y	9	3	Y	10	6	3	Y	4	3	Y	13	4	3	Y	6	0	N	3	1	N	10	2	3	Y	6	3	Y	2	3	Y	22	12	3	Y	16	3	Y	10	6	3	Y	4	3	Y	21	25	0	N
	CO				CO1			CO2				CO1			CO2				CO2			CO3			CO4				CO2			CO3			CO4				CO4			CO5				CO4			CO5				SEE	
	Number of Not Attempted(NA)					0			0				0			0				0			0			0				0			0			0				0			0				0			0				0
	Score index & No of Y's				2.9	101		2.9	99			3.0	105		3.0	105			3.0	78		2.0	67			64			3.0	105		3.0	105		3	105			3.0	105		3.0	105			3.0	105		3.0	105			0.8	7
	No. of N's					4			6				0			0				0			38			41				0			0			0				0			0				0			0				98
	CO Attainment					96.2			94.3				100			100				100			63.8			61				100			100			100				100			100				100			100				6.67
	Level					3			3				3			3				3			3							3			3							3			3				3			3				0

CO	CIE	SEE	DIRECT ATTAINMENT	Level	INDIRECT ATTAIN	Final Att
CO1	98.10	6.7	52.38	1.0	3.0	1.2
CO2	98.57	6.7	52.62	1.0	3.0	1.2
CO3	81.90	6.7	44.29	0.0	3.0	0.3
CO4	90.24	6.7	48.45	0.0	3.0	0.3
CO5	100.00	6.7	53.33	1.0	3.0	1.2
AVERAGE						0.8

CO	Score index out of 3
CO1	1.86
CO2	2.23
CO3	1.39
CO4	1.90
CO5	1.90

					Co-Po Mapping Table									
CO'S	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3	1	_	_	_	_	_	_	_	2	_	_	3	3
CO2	3	1	_	_	2	_	_	_	_	_	_	_	3	3
CO3	3	3	_	_	2	_	_	_	_	_	_	_	3	3
CO4	3	3	_	_	2	_	_	_	_	_	_	_	3	3
CO5	3	3	3	_	1	_	_	_	_	_	_	_	3	3
AVG	3.00	2.2	3.0	_	1.75	_	_	_	_	2.0	_	_	3.0	3.0

PO Attainment

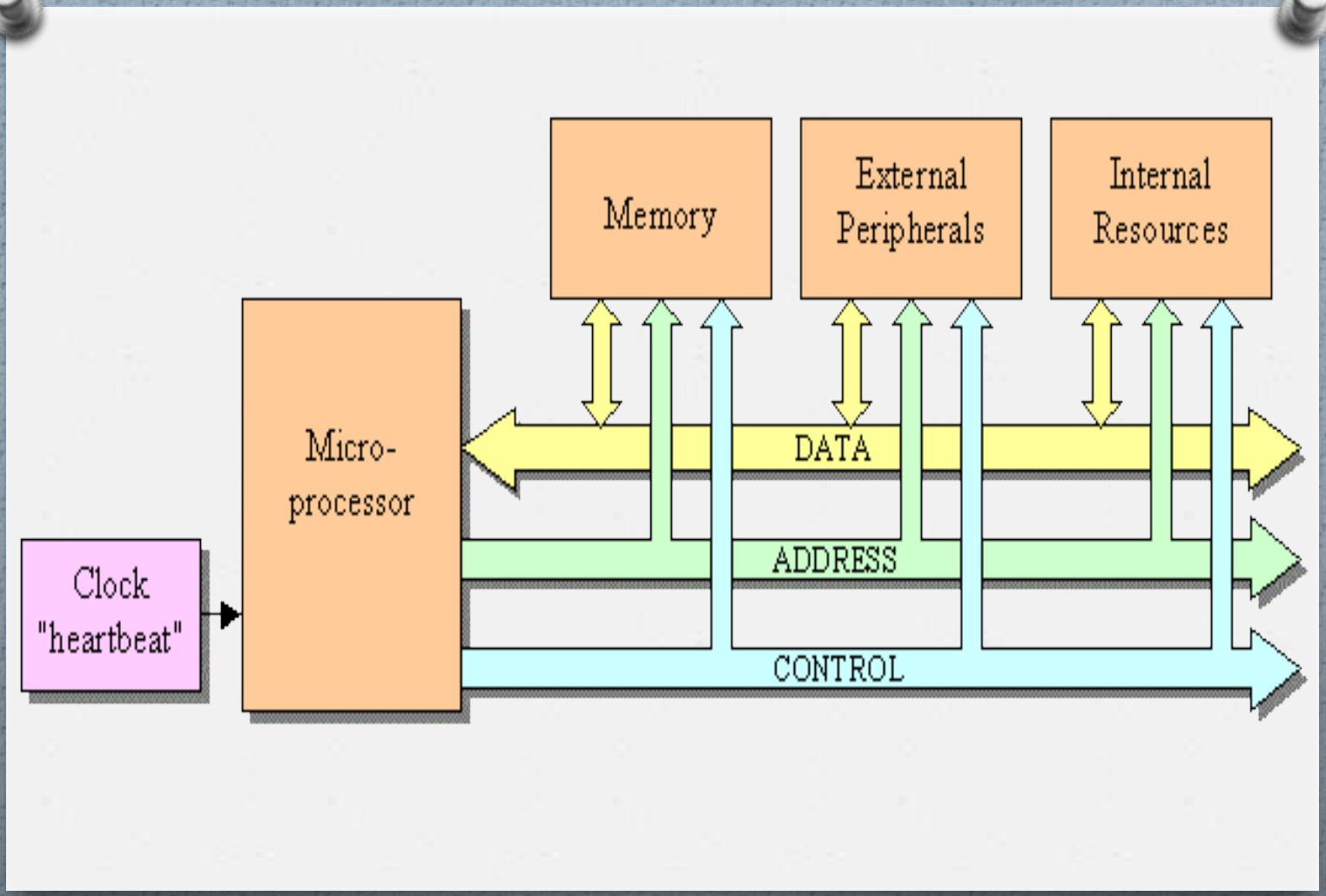
CO'S	CO Attainment	CO RESULT	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	1.20	N	1.20	0.4	_		_	_	_	_	_	0.80	_	_	1.20	1.20
CO2	1.20	N	1.20	0.4	_		0.8	_	_	_	_	_	_	_	1.20	1.20
CO3	0.30	N	0.3	0.3	_		0.2	_	_	_	_	_	_	_	0.30	0.3
CO4	0.30	N	0.3	0.3	_		0.2	_	_	_	_	_	_	_	0.30	0.3
CO5	1.20	N	1.20	1.20	1.20		0.4	_	_	_	_	_	_	_	1.20	1.20
Average			**0.8**	**0.5**	**1.2**		**0.4**	**_**	**_**	**_**	**_**	**0.8**	**_**	**_**	**0.8**	**0.8**

MICROCONTROLLER-18EC46

IA Marks:	40
Exam Marks:	60
Exam Hours:	03
Credits:	03

Text Book:

1. "The 8051 Microcontroller and Embedded Systems – using assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth J. Ayala, 3rd Edition, Thomson/Cengage Learning.



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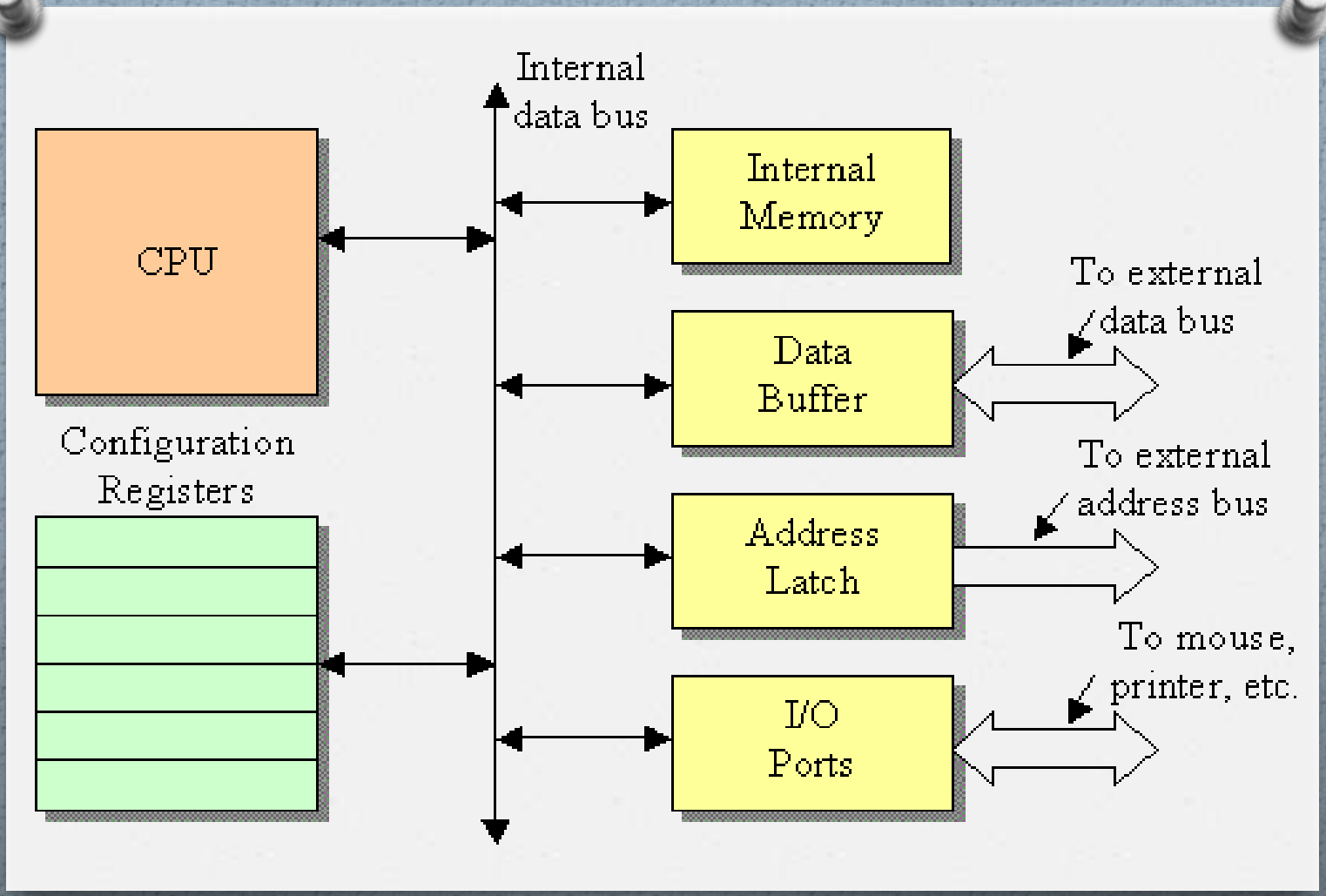

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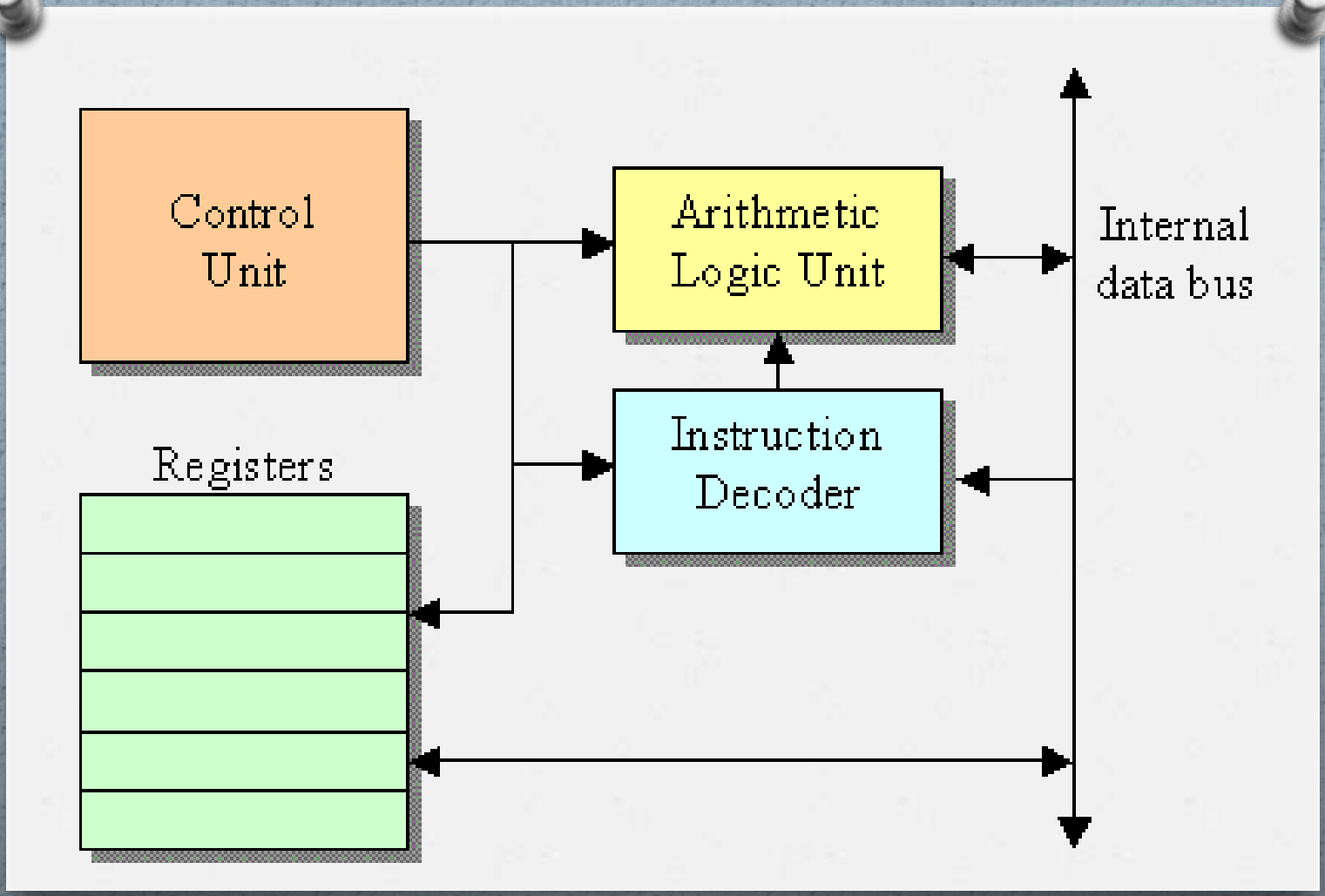

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Difference Between MP & MC

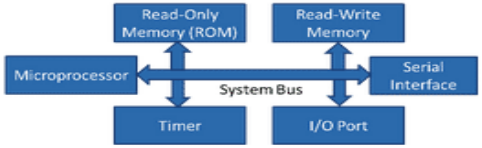
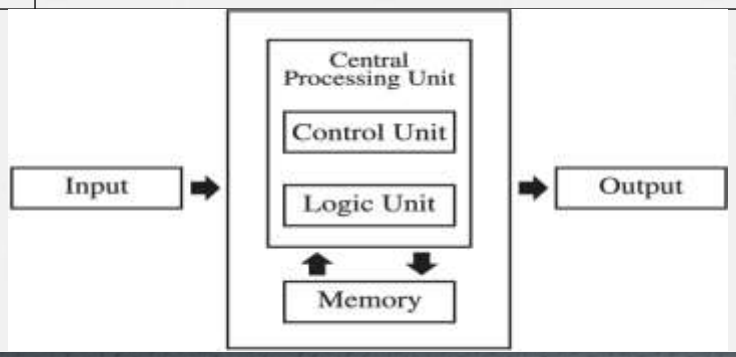
Microprocessor	Micro Controller
	
Microprocessor is heart of Computer system.	Micro Controller is a heart of embedded system.
It is just a processor. Memory and I/O components have to be connected externally	Micro controller has external processor along with internal memory and i/O components
Since memory and I/O has to be connected externally, the circuit becomes large.	Since memory and I/O are present internally, the circuit is small.
Cannot be used in compact systems and hence inefficient	Can be used in compact systems and hence it is an efficient technique
Cost of the entire system increases	Cost of the entire system is low
Due to external components, the entire power consumption is high. Hence it is not suitable to used with devices running on stored power like batteries.	Since external components are low, total power consumption is less and can be used with devices running on stored power like batteries.
Most of the microprocessors do not have power saving features.	Most of the micro controllers have power saving modes like idle mode and power saving mode. This helps to reduce power consumption even further.
Since memory and I/O components are all external, each instruction will need external operation, hence it is relatively slower.	Since components are internal, most of the operations are internal instruction, hence speed is fast.
Microprocessor have less number of registers, hence more operations are memory based.	Micro controller have more number of registers, hence the programs are easier to write.
Microprocessors are based on von Neumann model/architecture where program and data are stored in same memory module	Micro controllers are based on Harvard architecture where program memory and Data memory are separate
Mainly used in personal computers	Used mainly in washing machine, MP3 players

Image Source: https://www.electronicsforu.com

Difference Between MP & MC

Sl. No.	MICROPROCESSOR	MICROCONTROLLER
1	MP have many operational codes for moving data from external memory to the CPU	MC may have one or two
2	MP may have one or two bit handling instructions	MC will have many
3	Less multifunction pins on IC	Many multifunction pins on IC
4	MP takes many instructions to read and write data from external memory	MC takes few instructions to read and write data from external memory
5	Generally higher core clock frequency	Generally lower core clock frequency
6	High performance pipelined CPU Architecture	Low performance pipelined CPU Architecture
7	General purpose processor	Application specific single chip solution

Sl. No.	VON NEWMANN ARCHECITECTURE	HARWARD ARCHECITECTURE
1	The data and program are stored in the same memory	The data and program memories are separate
2	The code is executed serially and takes more clock cycles	The code is executed in parallel through pipeline and takes less clock cycles
3	The program can be optimized in lesser size	The program tend to grow big in size
4	One can't access program memory and data memory simultaneously	One can access program memory and data memory simultaneously



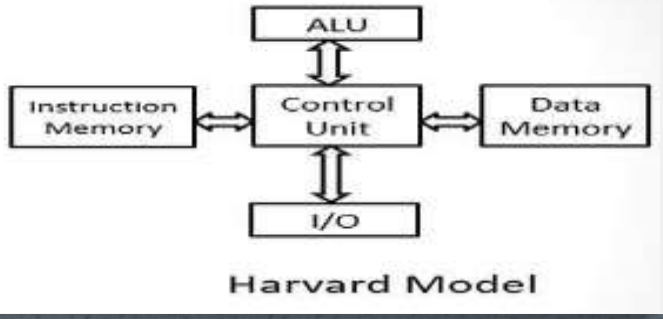


Image Source: https://www.researchgate.net/
https://www.quora.com/

Microcontroller for Embedded Systems

- MP and MC are widely used in embedded system products.
- An embedded product uses a MP or MC to do one task and one task only.
- Critical needs of an embedded system is to decrease power consumption and space.-> achieved by integrating more functions into the CPU chip

Examples of Embedded Systems

Home: Appliances, Sewing Machines, Cable TV Tuner, Remote Controls, Cellular Phones, Musical Instruments, Exercise Equipment

Office: Telephones, Fax Machines, Printers, Security Systems, Broadband Modem

Auto: Trip Computer, Engine Control, Air Bag, ABS, Transmission Control, Keyless Entry

Criteria for Choosing a Microcontroller

1. MC must meet the task at hand efficiently and cost effectively
   a. Speed. Highest Speed?
   b. Packaging. DIP or QFP ->space, assembling, and prototyping the end product
   c. Power Consumption. Critical for battery-powered products
   d. The amount of RAM and ROM on chip
   e. The number of I/O pins and the timer on the chip
   f. How easy it is to upgrade to higher performance or lower power consumption versions
   g. Cost per unit

2. How easy it is to develop products around it. The availability of an assembler, debugger, compiler, emulator, technical support.

3. Ready availability in needed quantities both now and in the future.-> more important than first two criteria.

Characteristic features of 8051-Microcontroller

Image Source: https://en.wikipedia.org/
https://www.geeksforgeeks.org

- 8051 is an 8-bit microcontroller, The ALU performs one 8-bit operation at a time
- 8-bit data bus
- 16-bit address bus, The 16 bit address bus can address a 64K(2^{16}) byte code memory space and a separate 64K byte of data memory space
- 8051 has 4K on-chip read only code memory (ROM)
- 128 bytes of internal Random Access Memory (RAM)
- There are 34, 8-bit general purpose registers
- There are 21 SFRs.
- Two 16-bit timers/ counter
- Four 8-bit I/O ports (3 of them are dual purpose). One of them used for serial port
- 5+1 Interrupts are there: 2 timer interrupts, 2 external hardware interrupts and one serial interrupt
- 8051 is a 40 pin IC

PIN Details of 8051-Microcontroller

40 pins of the 8051 chip:

Most of these pins are used to connect to I/O devices or external data and code memory

1. Four I/O port take 32 pins(4 x 8 bits)
2. A pair of Vcc and GND pins for power supply (the 8051 chip needs +5V 500mA to function properly)
3. A group of pins (EA, ALE, PSEN) for internal and external data and code memory access controls
4. A pair of Crystal clock pins(XTAL1,2)
5. One Reset pin for reboot purpose. Referred as power-on reset, on reset will cause all values in the register to be lost, PC=0

4. System Clock and Oscillator Circuits

- The 8051 requires an external oscillator circuit. The oscillator circuit usually runs around 12MHz.
- The crystal generates 12M pulses in one second. The pulse is used to synchronize the system operation in a controlled pace.
- A machine cycle is minimum amount time a simplest machine instruction must take.
- An 8051 machine cycle consists of 12 crystal pulses (ticks).
- Instruction with a memory operand needs multiple memory accesses(machine cycles).
- The first 6 crystal pulses (clock cycle) is used to fetch the opcode and the second 6 pulses are used to perform the operation on the operands in the ALU.
- This gives an effective machine cycle rate at 1MIPS (Million Instructions Per Second).

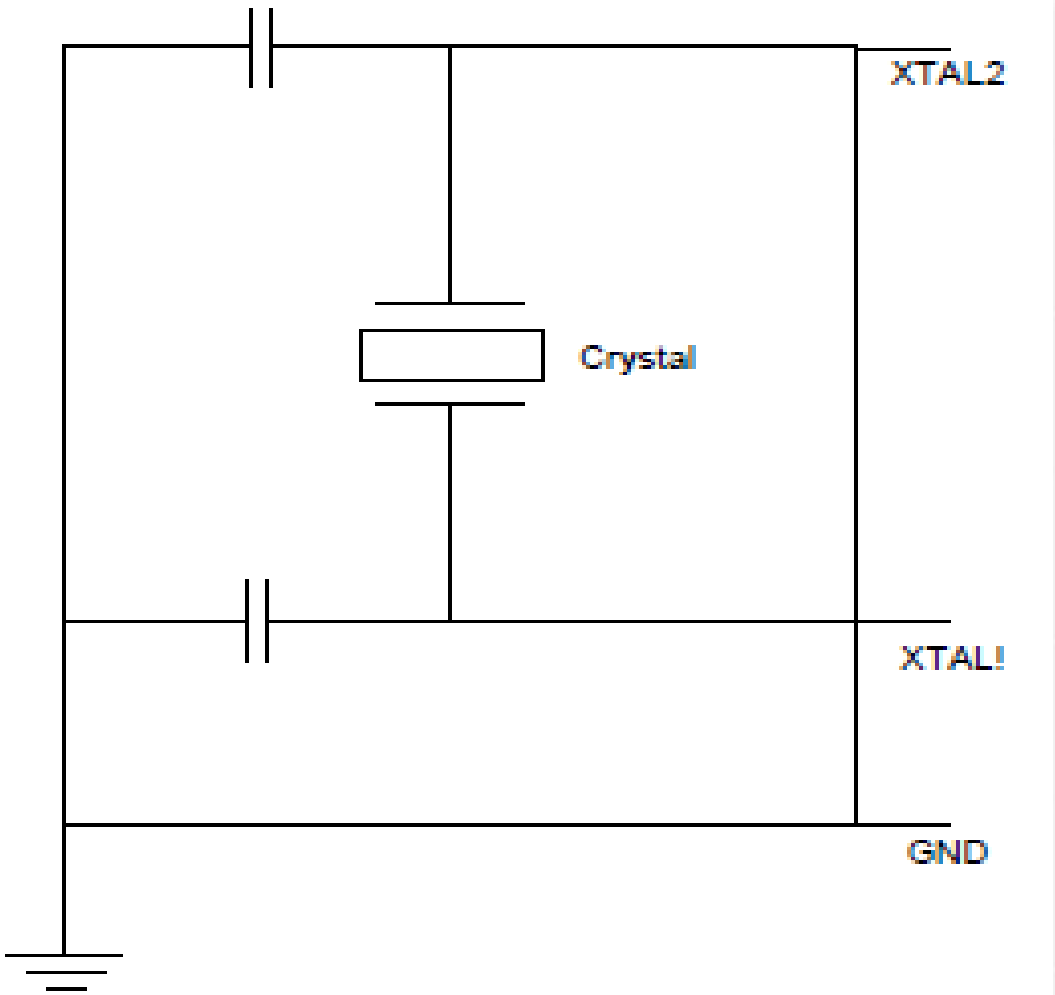


Image Source: https://www.google.com/

1. Ports 0,1,2 and 3

- P0 is also designated as AD0 – AD7, allowing it to be used for both address and data
- When connecting to an external memory, P0 provides both address and data
- The 8051 multiplexes address and data through P0 to save pins
- ALE indicates if P0 has address or data
- When ALE=0, it provides data D0-D7, but when ALE=1 it has address A0-A7
- Thus ALE is used for demultiplexing address and data with the help of a 74LS373 latch IC

- When there is no external memory connection, pins of P0 must be connected externally to 10k ohm pull-up resistor
- Because P0 is an open drain, unlike P1,P2 and P3
- When connected to pull-up resistors P0 can be used as a simple I/O port, just like P1 and P2
- In contrast P1,P2 and P3 do not need any pull-up resistors since they already have pull-up resistors internally
- Upon reset, ports P1,P2 and P3 are configured as input ports

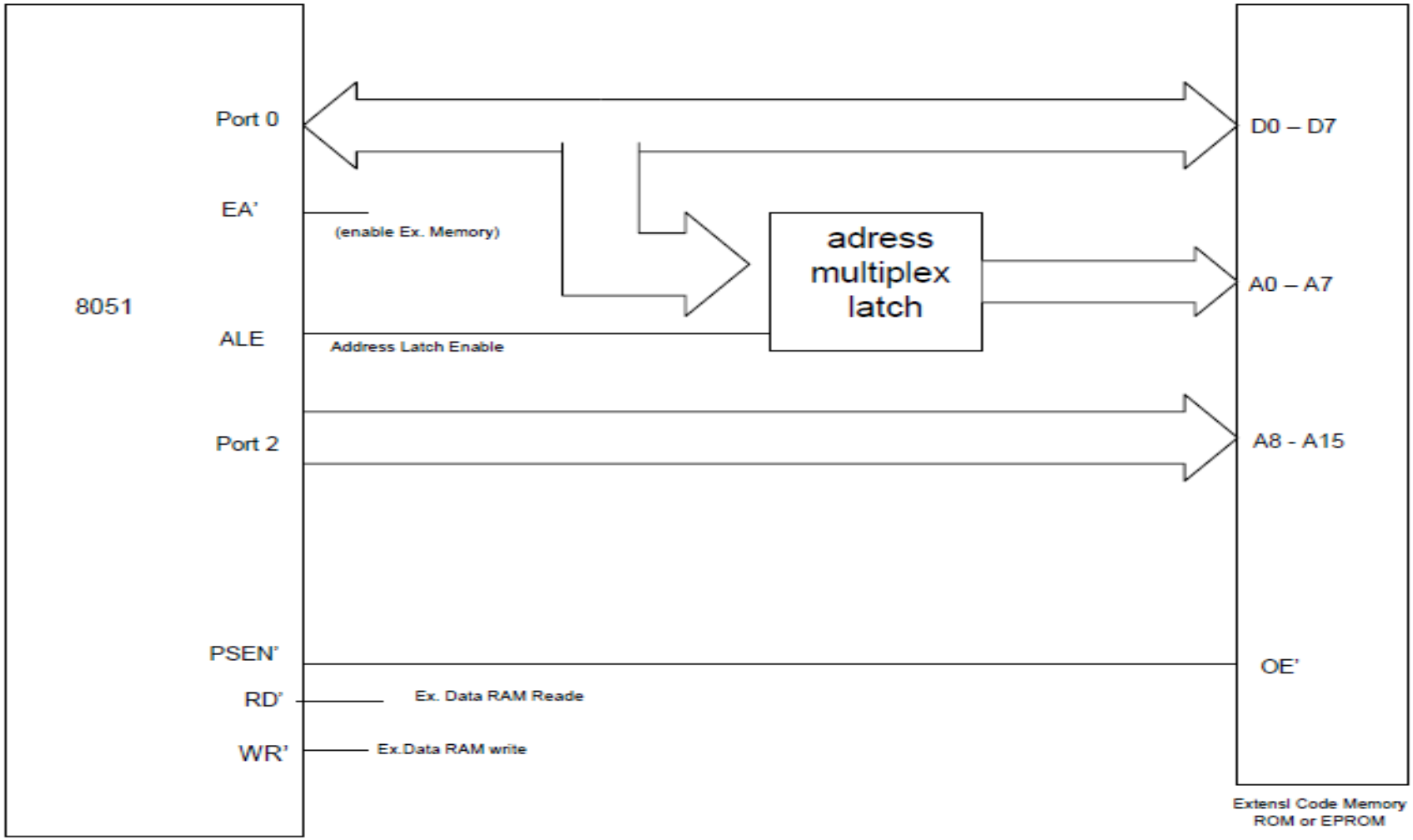
Ports1 and 2

- With no external memory connection, both P1 and P2 are used as simple I/O ports
- With external memory connection, P2 must be used along with P0 to provide the 16-bit address for the external memory
- P2 is also designated as A8-A15, indicating its dual function
- P2 is used for the upper 8 bits of the 16-bit address, and it cannot be used for I/0

Ports 3

- Can be used as an input or output
- Does not need pull-up resistors
- Configured as an input port upon reset, this is not the way it is most commonly used
- P3 has the additional function of providing extremely important signals such as interrupts
- P3.0 and P3.1 are used for the RxD and TxD serial communication signals
- Bits P3.2 and P3.3 are set aside for external interrupts
- Bits P3.4 and P3.5 are used for Timers 0 and 1
- Bits P3.6 and P3.7 are used to provide the WR and RD signals of external memory connections

3. External data and code memory access



The Pin Connection for External Code and Data Memory

- EA’ (31) is an input pin and is connected to either Vcc or GND, it cannot be unconnected.
- The EA' (External Access) pin is used to control the internal or external memory access.
- The signal 0 is for external memory access and signal 1 for internal memory access.
- PSEN’ is an output pin.
- The PSEN' (Program Store Enable) is for reading external code memory when it is low (0) and EA is also 0.
- ALE is an output pin.
- The ALE (Address Latch Enable) activates the port 0 joined with port 2 to provide 16 bit external address bus to access the external memory.
- The ALE demultiplexes the P0: 1 for latching address on P0 as A0-A7 in the 16 bit address bus, 0 for latching P0 as data I/O.

- P0.x is named ADx because P0 is multiplexed for Address bus and Data bus at different clock time.
- WR' provides the signal to write external data memory
- RD' provides the signal to read external data and code memory.

Memory Capacity and Memory Organization

- The number of bits that a semiconductor memory chip can store is called memory capacity
- It can be in units of Kbits (kilobits), Mbits (megabits) and so on- eg: 16M memory chip – 16 megabits
- Where as memory capacity of a computer system is given in bytes- eg: 16M memory – 16 megabytes
- Memory chips are organized into a number of locations within the IC
- Each location can hold 1 bit, 4 bits, 8 bits, or even 16 bits, depending on how it is designed internally

- The number of locations within a memory IC depends on the address pins
- The number of bits that each location can hold is always equal to the number of data pins
- A memory chip contain 2^x location, where x is the number of address pins
- Each location contains y bits, where y is the number of data pins on the chip
- The entire chip will contain $2^x \times y$ bits - Memory organization

- Example: A given memory chip has 12 address pins and 4 data pins. Find: (a) The organization, and (b) the capacity.

Solution: (a) This memory chip has 4096 locations ($2^{12} = 4096$), and each location can hold 4 bits of data. This gives an organization of 4096×4, often represented as $4K \times 4$.

(b) The capacity is equal to 16K bits since there is a total of 4K locations and each location can hold 4 bits of data

- A 512K memory chip has 8 pins for data. Find: (a) The organization, and (b) the number of address pins for this memory chip.

Solution: (a) A memory chip with 8 data pins means that each location within the chip can hold 8 bits of data. To find the number of locations within this memory chip, divide the capacity by the number of data pins. 512K/8 = 64K; therefore, the organization for this memory chip is $64K \times 8$

(b) The chip has 16 address lines since $2^{16} = 64K$

Memory Address Decoding

Memory pins have one or more pins called CS (Chip Select), which must be activated for the memory contents to be accessed. It is also called chip enable (CE)

To connect a memory chip to the CPU/Microcontroller:

- The data bus of the MC is connected directly to the data pins of the memory chip
- Control signals RD! and WR! From the MC are connected to the OE (output enable) and WE (write enable) pins of the memory chip respectively
- In case of the address buses, the lower bits of the addresses from the MC go directly to the memory chip address pins

- While the upper ones are used to activate the CS pin of the memory chip
- No data can be written into or read from the memory chip unless CS is activated
- The CS input of a memory chip is normally active low and is activated by the output of the memory decoder
- Normally memories are divided into blocks and the output of the decoder selects a given memory block
- There are 3 ways to generate a memory block selector

Three ways to generate memory block Selector

1. Using simple logic gates
2. Using the 74LS138 IC
3. Using programmable logics

1. Using simple logic gates

Using NAND gate is the simplest method of decoding because output of NAND gate is active low and that of CS pin is also active low

3000 to 3FFF
0011 0000 0000 0000 to 0011 1111 1111 1111

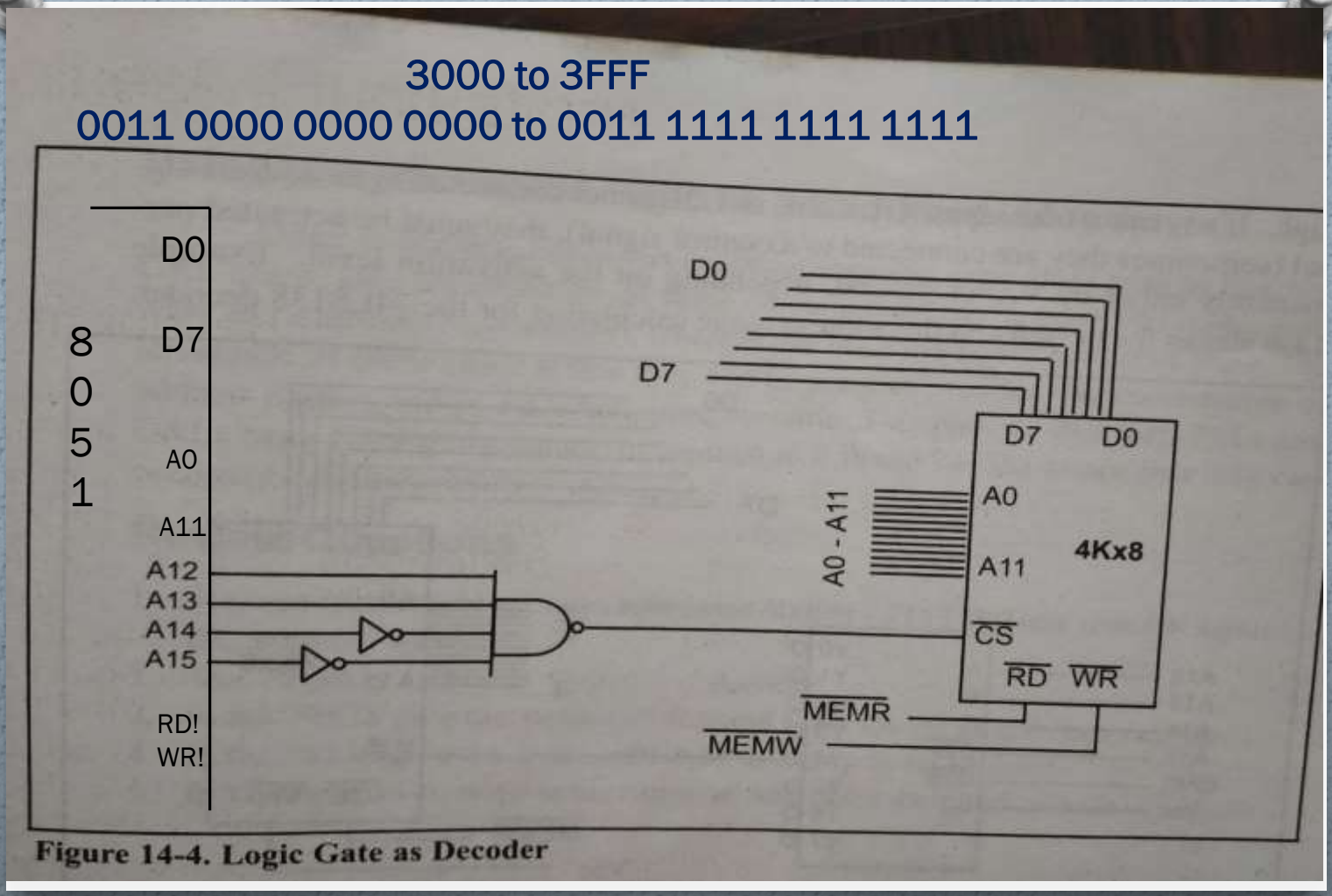


Figure 14-4. Logic Gate as Decoder

2. Using the 74LS138 IC

- Most widely used address decoders
- The 3 inputs A, B & C generate 8 active low outputs Y0 to Y7
- Each Y output is connected to CS of a memory chips, allowing control of 8 memory blocks by a single 74LS138
- There are 3 additional inputs G2A!, G2B! & G1.
- If any one of these are not connected to an address signal, they must be activated permanently either by Vcc or GND, depending on the activation level

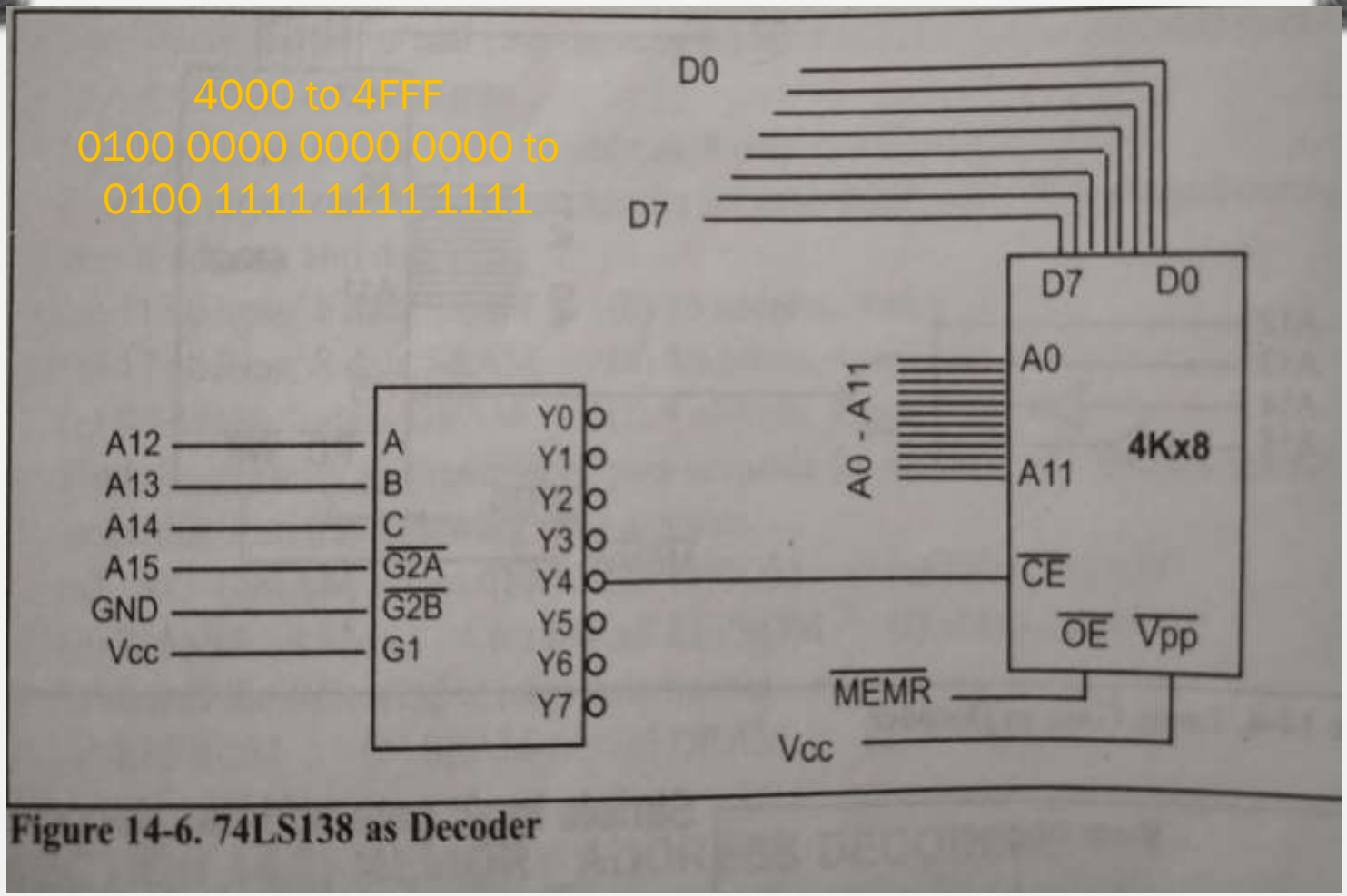


Figure 14-6. 74LS138 as Decoder

2. Using programmable logics

- Other widely used decoder are programmable logic chips such as PAL & GAL chips
- These are versatile since these can be programmed for any combination of address ranges
- These have 10 or more inputs in contrast to 6 in 74LS138 means that it can accommodate more address pins
- These need to have access to a PAL/GAL software and a programmer (burner)

Interfacing with External ROM

- The following pins are used in external memory interfacing:

1. External Access (EA!) Pin: is an input pin and is connected to either Vcc or GND, it cannot be left unconnected.

- when connected to Vcc the program code is stored in the Microcontroller on-chip ROM.
- when connected to GND, the program code is stored in external ROM.

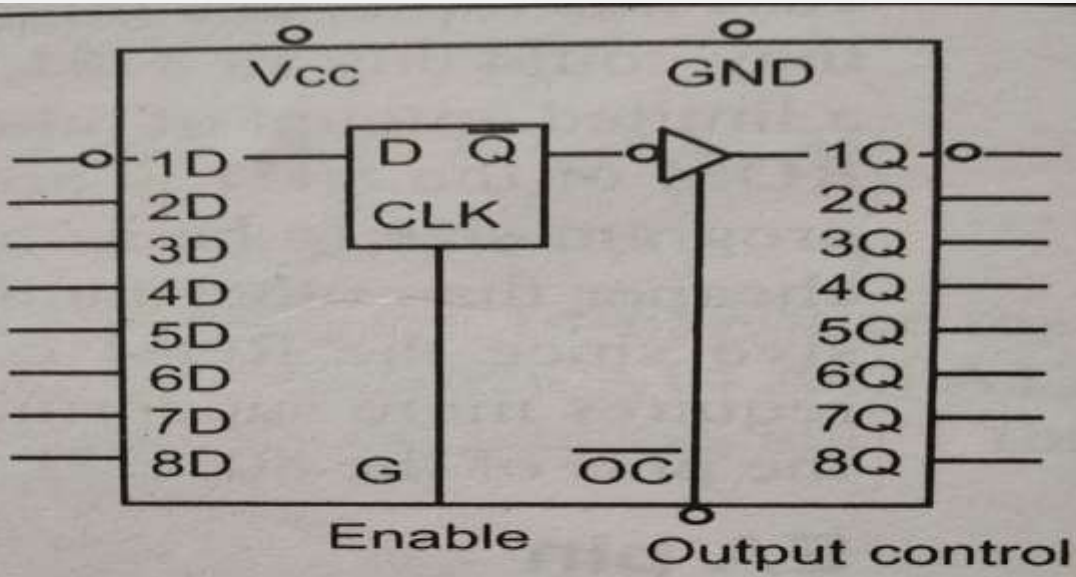
2. P0 & P2 role in Providing Address: P0 & P2 provide the 16 bit address to access 64Kbytes of external memory.

- P0 provides the lower 8-bit addresses A0-A7
- P2 provides the upper 8-bit addresses A8-A15
- More importantly, P0 is also used to provide the 8-bit data bus D0-D7
- It means P0 provides both address and data paths. This is called address/data multiplexing

3. ALE: is an output pin, when ALE=1, P0 is used for the address path and when ALE=0, P0 is used to send/receive data

- To extract the address from the P0 pin, we connect P0 to a 74LS373 latch IC, and use ALE pin to latch the address as shown in fig below:
- The extracting of address from P0 is called address/data demultiplexing

74LS373 D Latch



Funtion Table

Output control	Enable G	Enable D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Figure 14-8. 74LS373 D Latch
(Reprinted by permission of Texas Instruments, Copyright Texas Instruments, 1988)

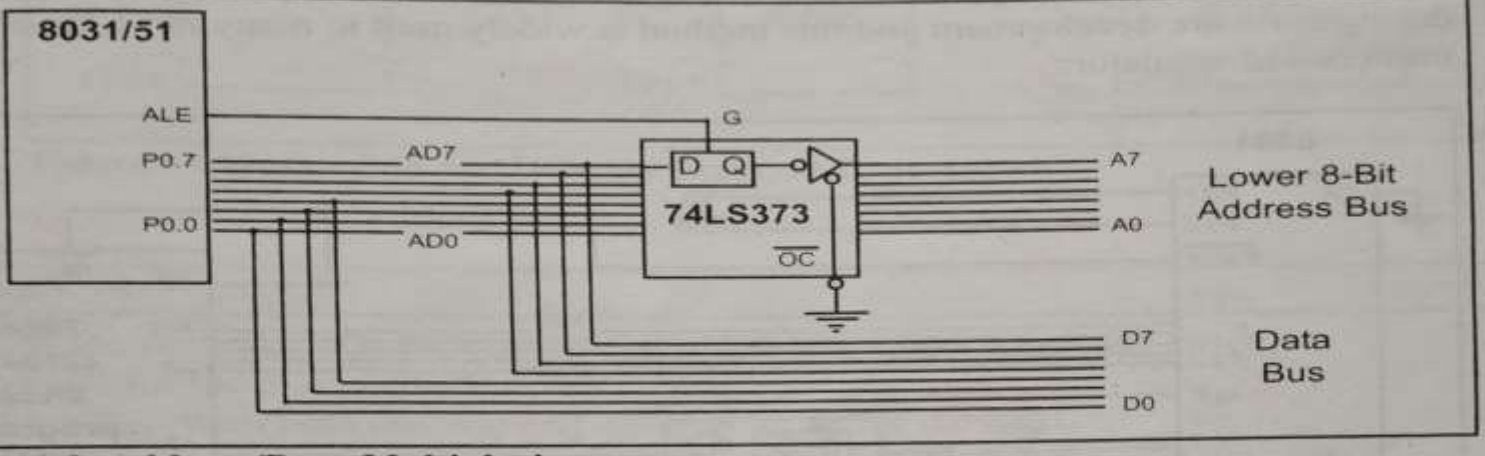


Figure 14-9. Address/Data Multiplexing

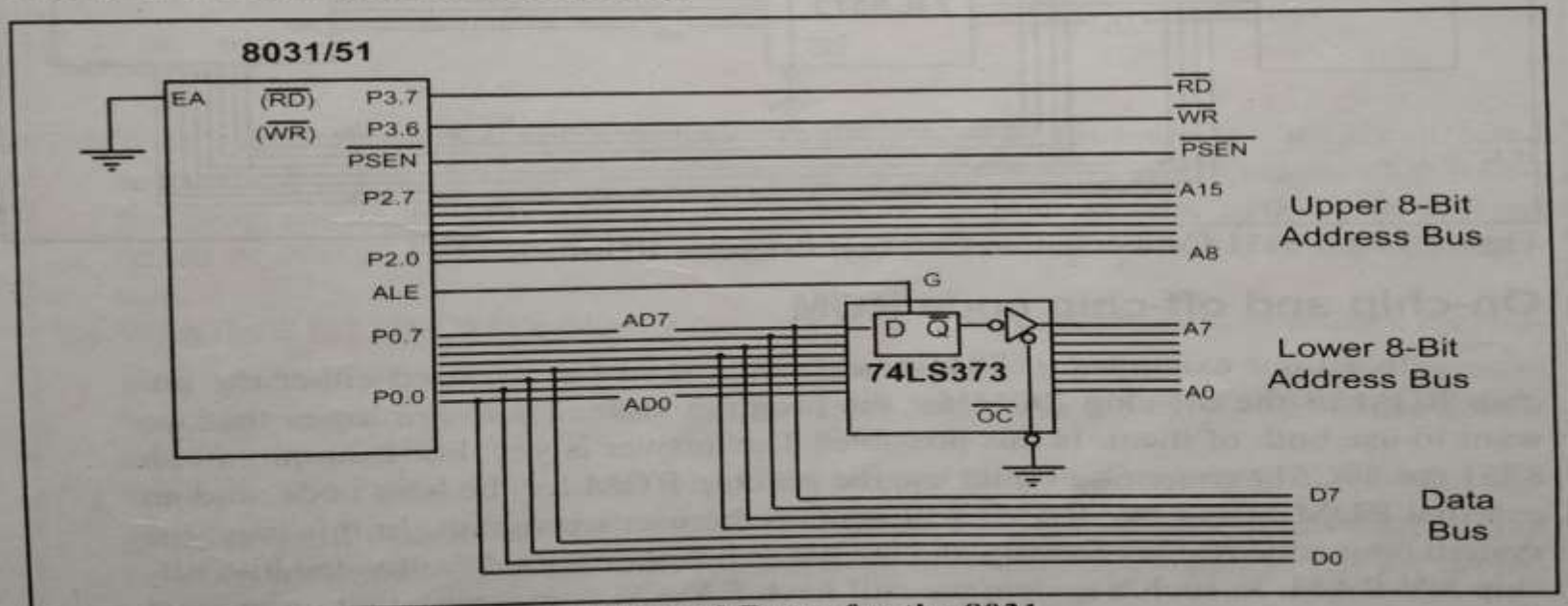


Figure 14-10. Data, Address, and Control Buses for the 8031
(For reset and crystal connection, see Chapter 4.)

4. Program Store Enable (PSEN!): is an output pin connected to the OE! Pin of a ROM

- To access external ROM containing program code, the 8051 uses the PSEN! Signal
- When EA! Pin connected to GND, the 8051 fetches opcodes from external ROM by using PSEN!,
- When EA! Pin is connected to Vcc, the 8051 do not activate the PSEN! Pin – this indicates that the on-chip ROM contains program code

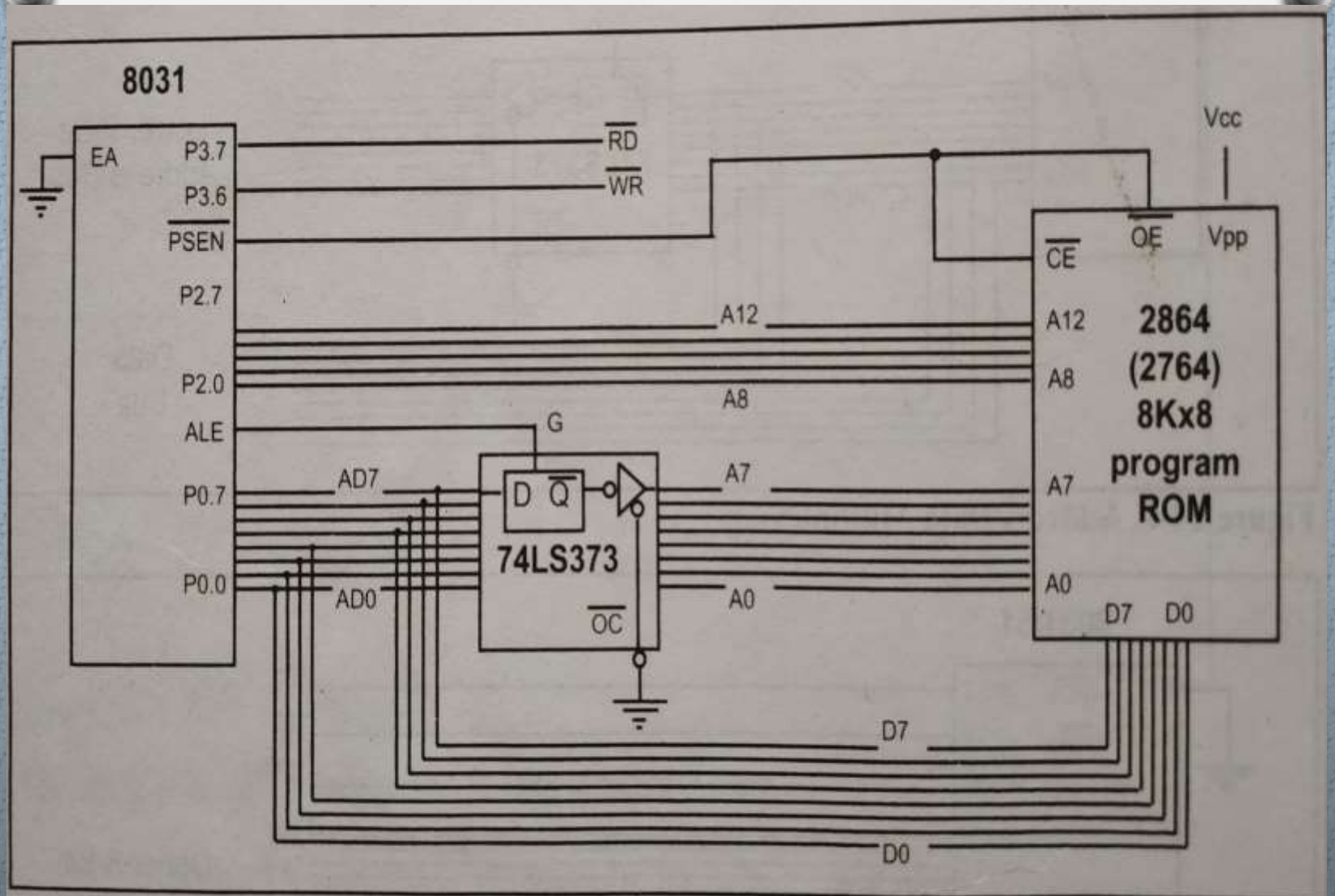


Figure 14-11. 8031 Connection to External Program ROM

On-Chip & Off-Chip Code ROM

- When system with both on-chip and off-chip ROM code and EA!=Vcc
- Controller fetches the opcode from 0000 to 0FFF (on-chip ROM) then the PC generates address 1000 (off-chip ROM)

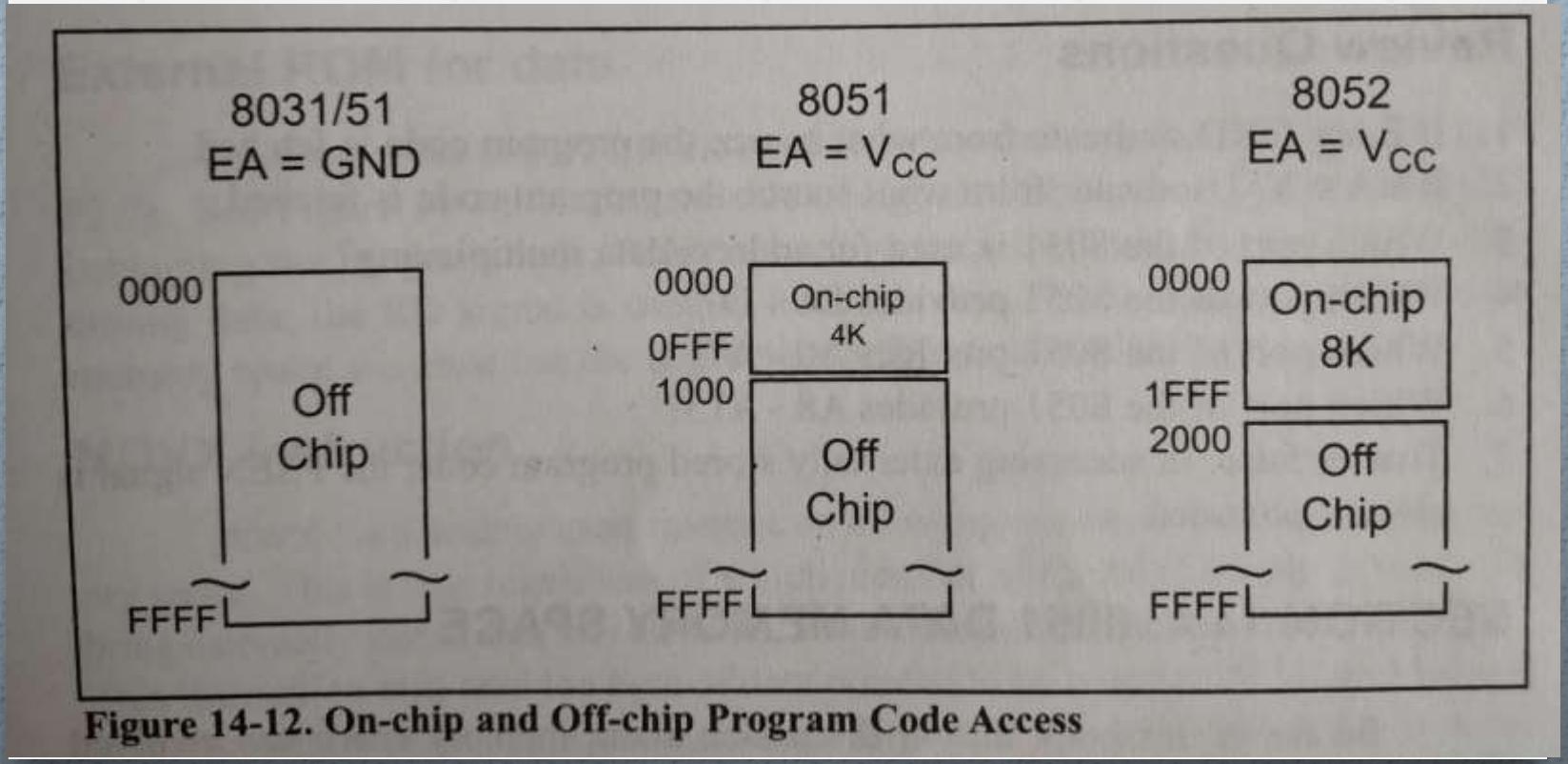


Figure 14-12. On-chip and Off-chip Program Code Access

Data Memory Space

- The 8051 has 128K bytes of address space of which 64K bytes are set aside for program code and the other 64K bytes are set aside for data
- Program space is accessed using the program counter (PC) to locate and fetch instructions
- Data memory space is accessed using the DPTR register and an instruction called MOVX
- X stands for external (meaning that the data memory space must be implemented externally)
- MOVX A, @DPTR - here DPTR (16) register holds the address of the data ROM
- For data ROM RD! pin is used instead of PSEN! Pin

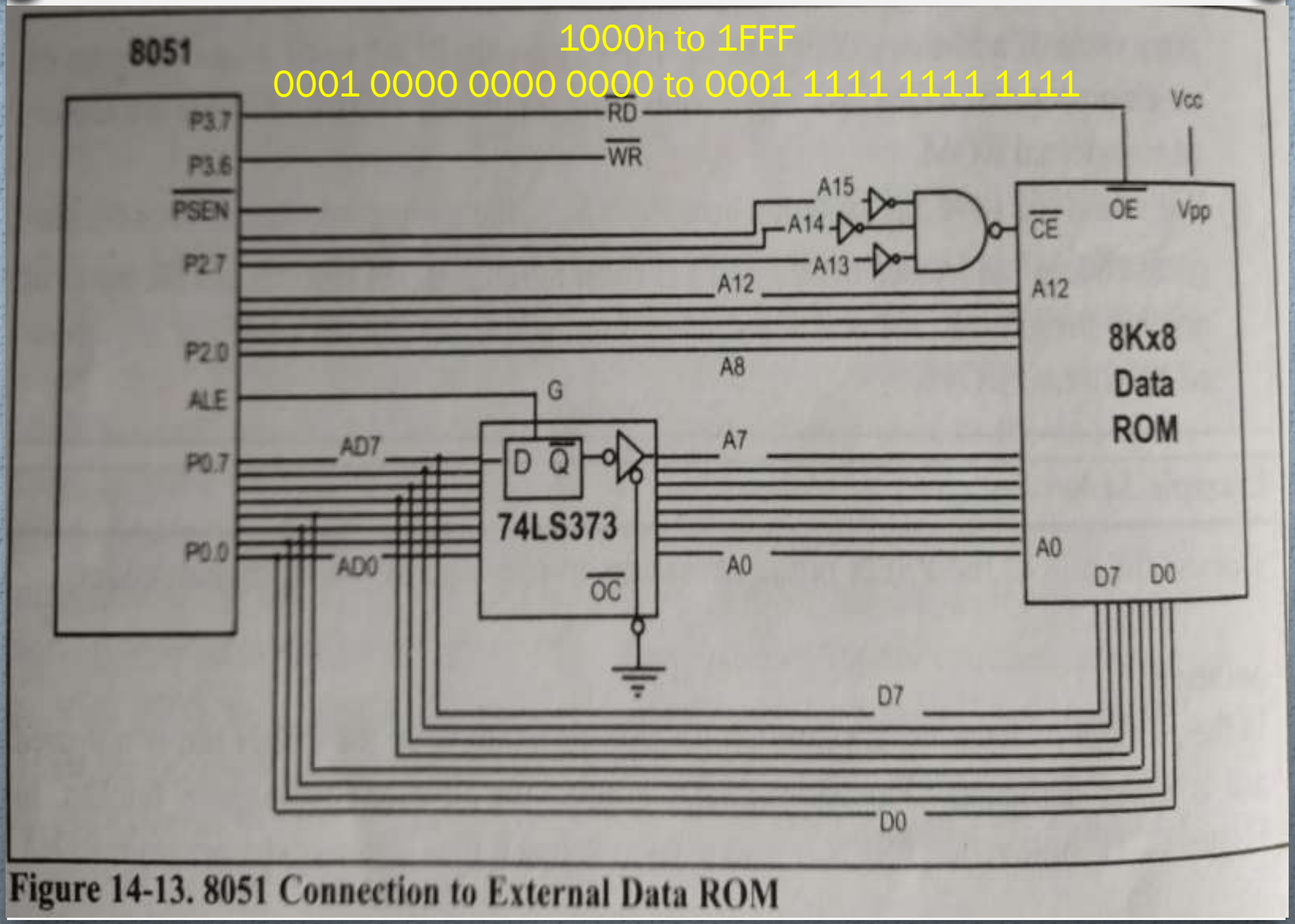


Figure 14-13. 8051 Connection to External Data ROM

Example 14-11

Show the design of an 8031-based system with 8K bytes of program ROM and 8K bytes of data ROM.

Solution:

Figure 14-14 shows the design. Notice the role of PSEN and RD in each ROM. For program ROM, PSEN is used to activate both OE and CE. For data ROM, we use RD to activate OE, while CE is activated by a simple decoder.

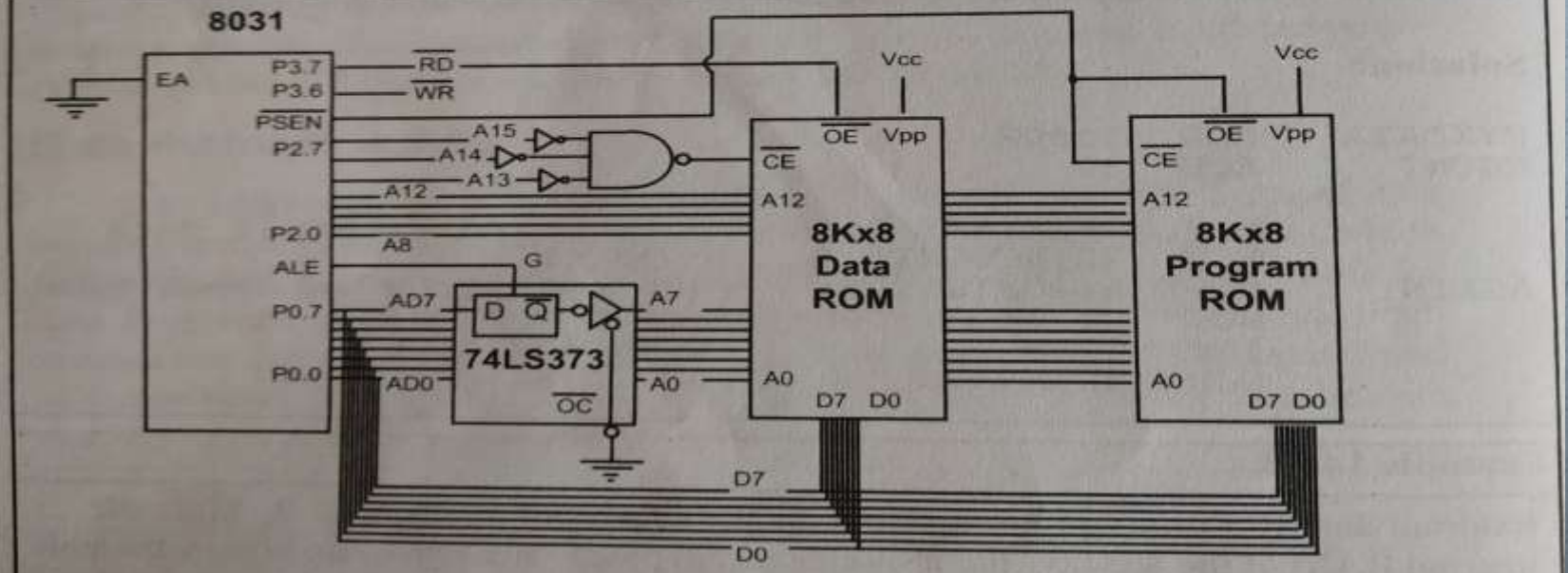


Figure 14-14. 8031 Connection to External Data ROM and External Program ROM

Interfacing of External Data RAM

- To connect to external RAM, we must use both RD! and WR! Pins
- In writing data to external data RAM, use the instruction MOVX @DPTR, A

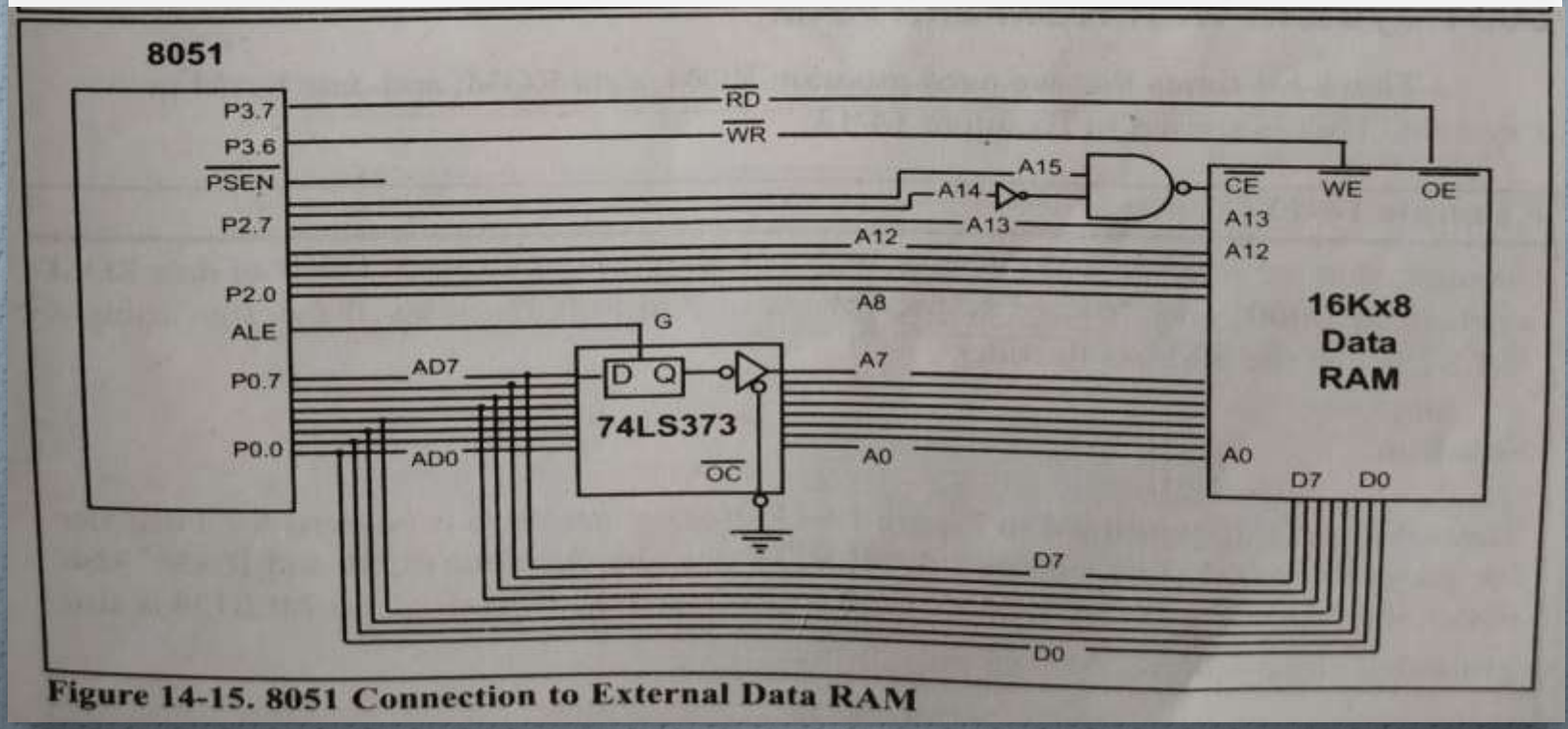


Figure 14-15. 8051 Connection to External Data RAM

A single external ROM for code and data

- A single ROM chip is used for both data and code of 64Kx8 capacity
- We know that PSEN! Is used to access the external code space and the RD! pin is used to access the external data space
- To allow a single ROM chip to provide both program code space and data space, use an AND gate to signal OE! Pin of the ROM chip as shown:

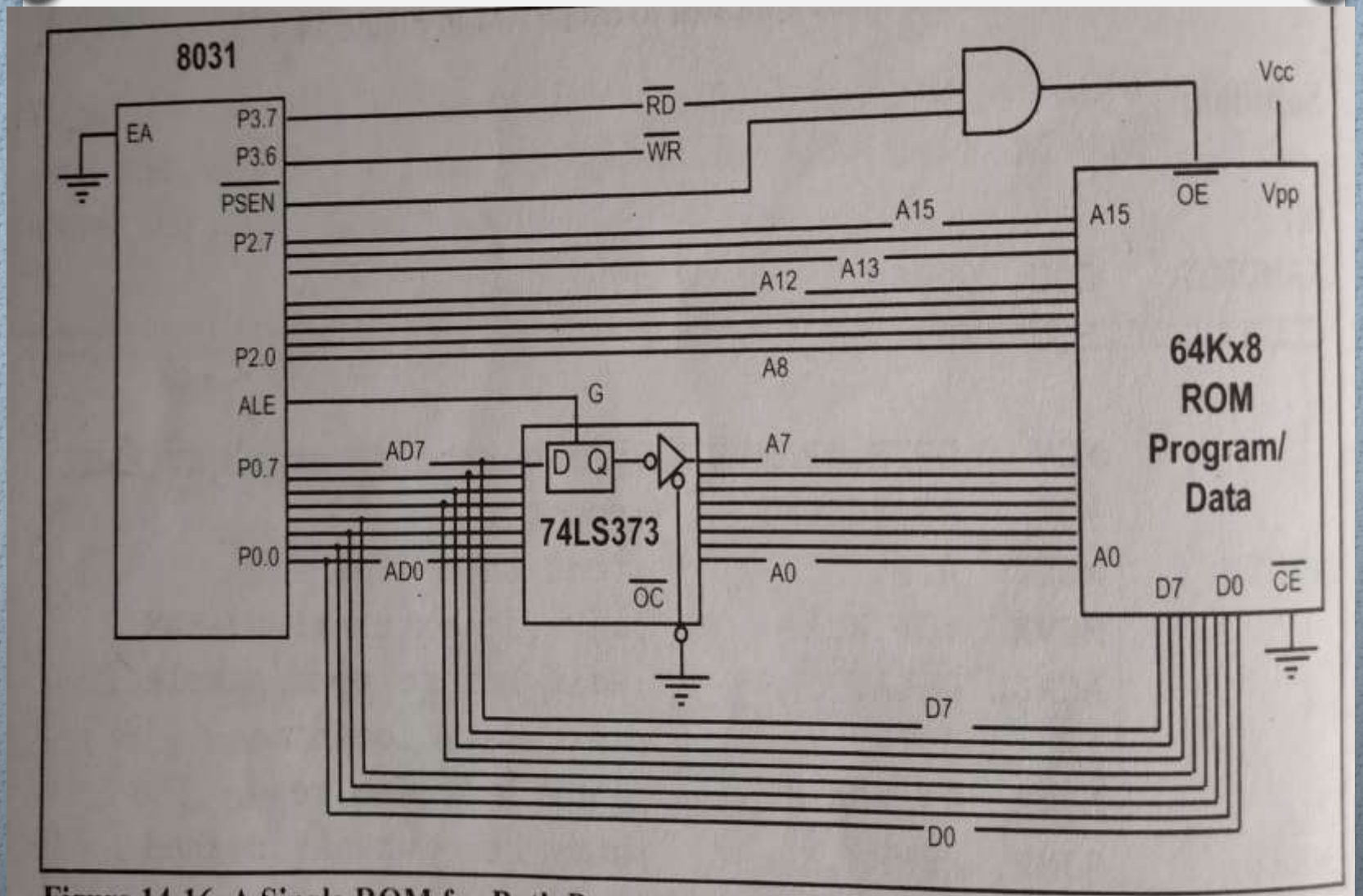


Figure 14-16. A Single ROM for Both Program and Data

Interfacing Program ROM, Data ROM and Data RAM

- No need for decoder for program ROM
- But require a 74LS138 decoder for data ROM and RAM
- Note that G1=Vcc, G2A!=GND, G2B!=GND and the C input is also grounded since we use only Y0 – Y3

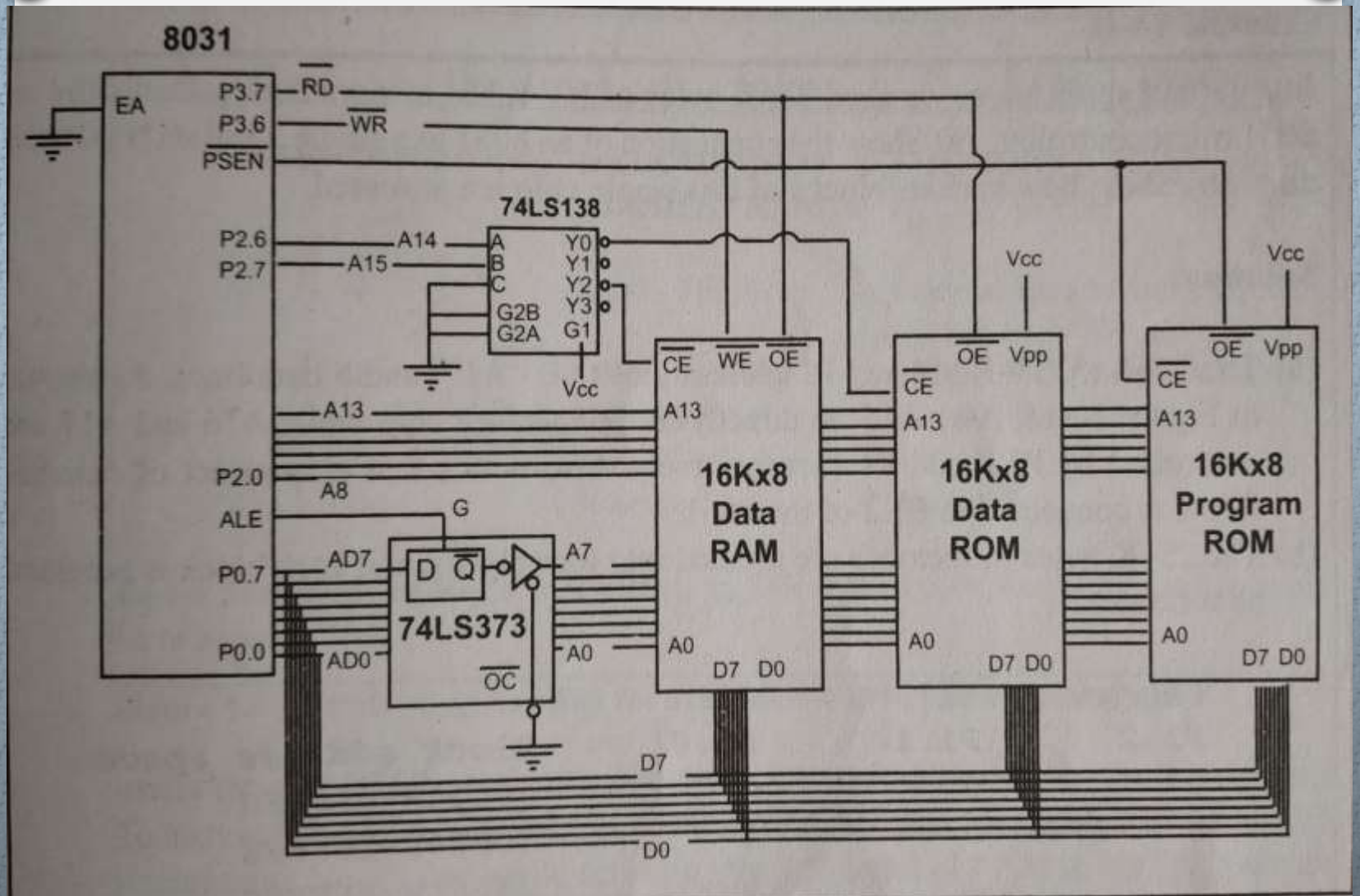


Figure 14-17. 8031 Connection to External Program ROM, Data RAM, and Data ROM

Interfacing to Large External Memory

- In some applications we need a large amount of memory to store data – 256K bytes
- But 8051 can support only 64K bytes of external data memory, since DPTR is 16-bit
- To solve this problem connect A0 – A15 of 8051 directly to the external memory's A0-A15 pins
- And use some of the P1 pins to access the 64K byte blocks inside the single 256Kx8 memory chip

Chip Select	A17	A16	
P1.2	P1.1	P1.0	Block Address Space
0	0	0	00000H – 0FFFFH
0	0	1	10000H – 1FFFFH
0	1	0	20000H – 2FFFFH
0	1	1	30000H – 3FFFFH
1	X	X	External RAM Disabled

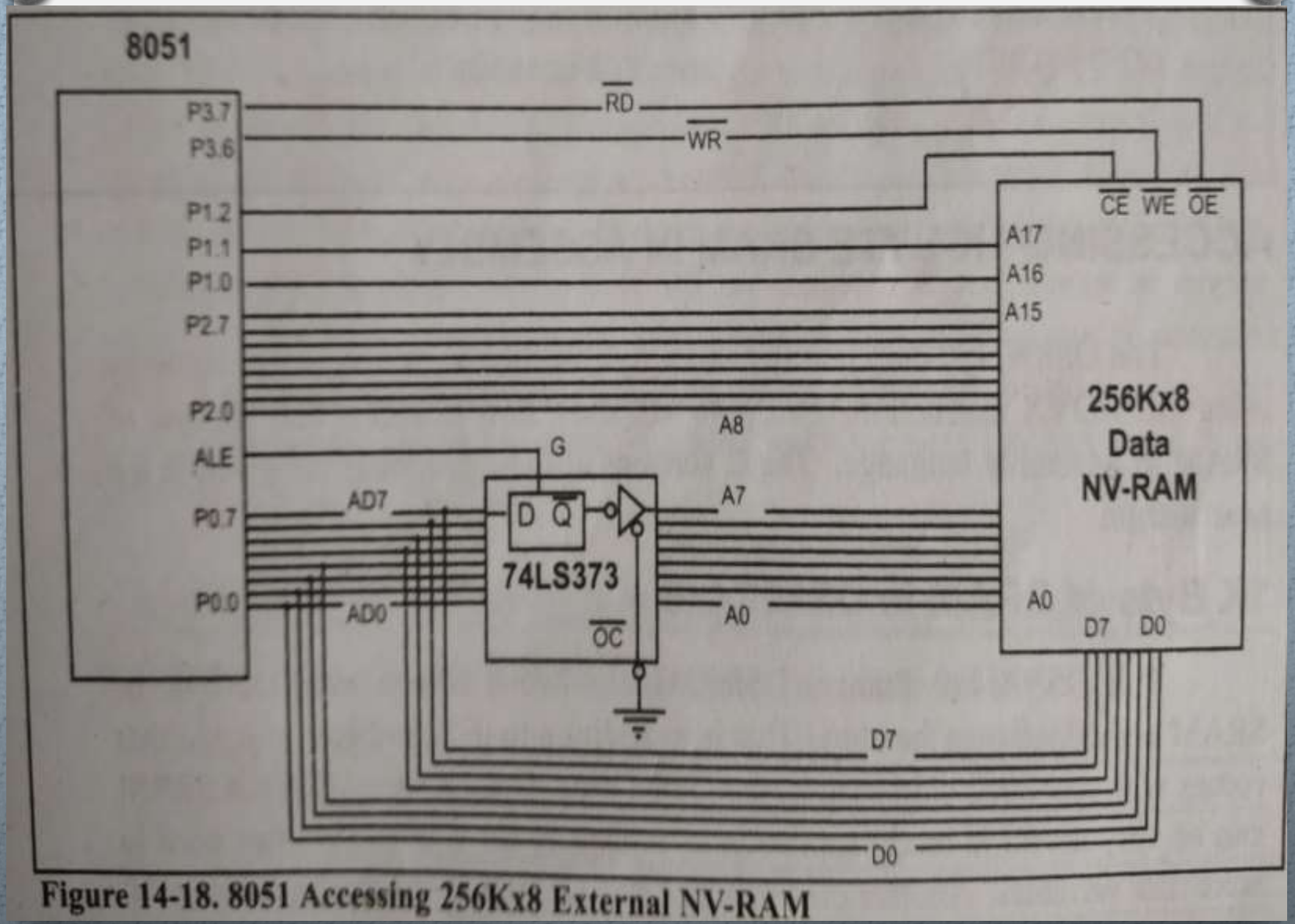
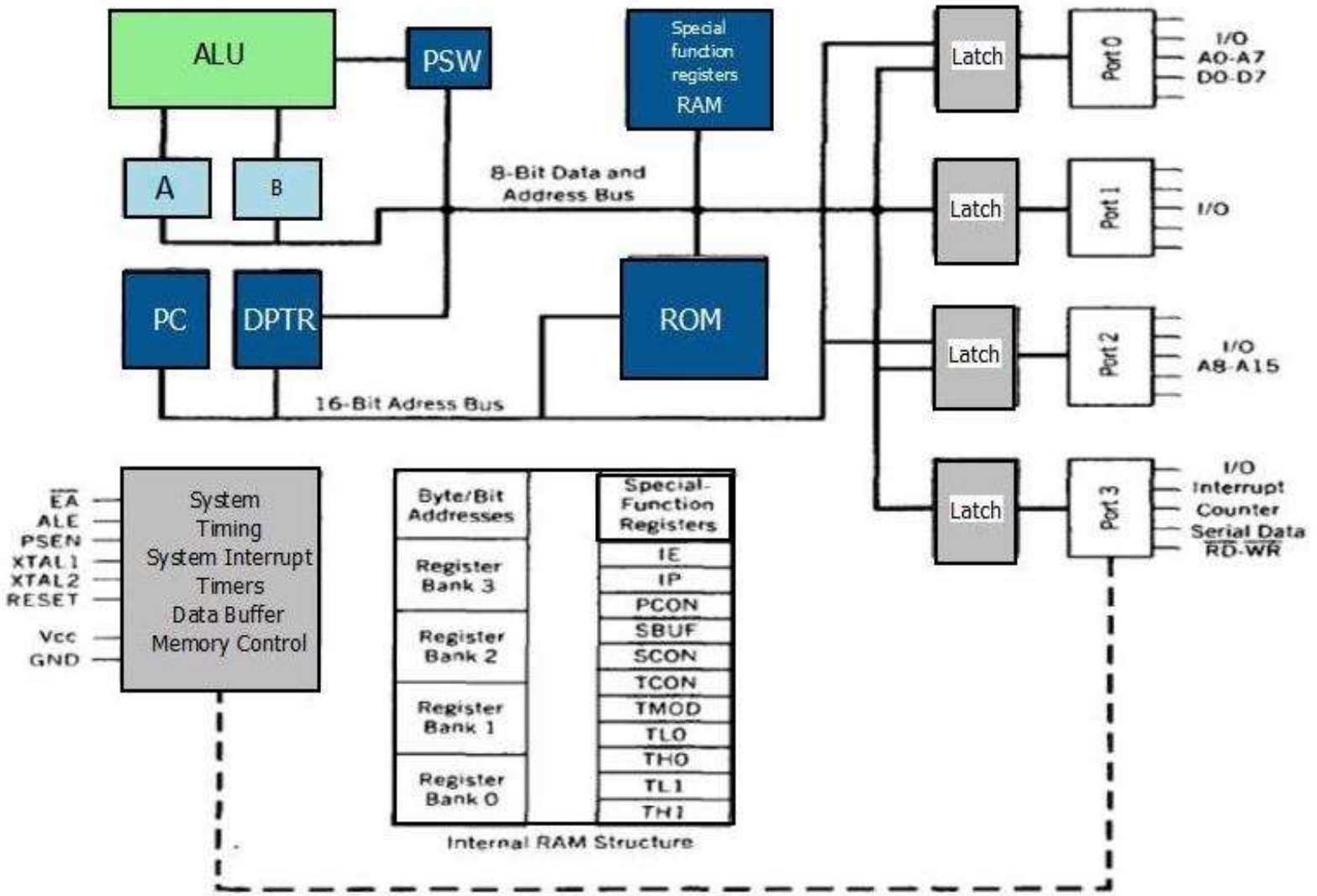


Figure 14-18. 8051 Accessing 256Kx8 External NV-RAM

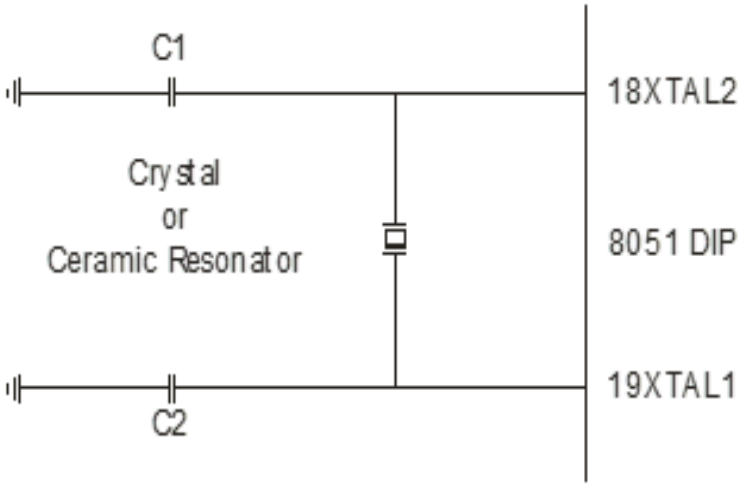
The 8051 Architecture

- To learn a new computer/ controller first one need to become familiar with the capability of the machine
- The features of the computer/ controller are best learned by studying the internal hardware design, also called the architecture of the device
- Architecture is learnt to determine the type, number and size of the registers and other circuitry


ALU
PSW
A
B
PC
DPTR
Special function registers RAM
ROM
8-Bit Data and Address Bus
16-Bit Adress Bus
Latch
Latch
Latch
Latch
Port 0
Port 1
Port 2
Port 3
I/O A0-A7 D0-D7
I/O
I/O A8-A15
I/O Interrupt Counter Serial Data RD-WR
EA
ALE
PSEN
XTAL1
XTAL2
RESET
Vcc
GND
System Timing System Interrupt Timers Data Buffer Memory Control
Byte/Bit Addresses
Special-Function Registers
Register Bank 3
Register Bank 2
Register Bank 1
Register Bank 0
IE
IP
PCON
SBUF
SCON
TCON
TMOD
TL0
TH0
TL1
TH1
Internal RAM Structure

The 8051 Oscillator and Clock

- The heart of the 8051 is the circuitry that generates the clock pulses by which all internal operations are synchronized
- Pins XTAL1 and XTAL2 are provided for connecting a resonant network to form an oscillator
- Quartz crystal and capacitors are employed as part of clock circuitry
- The crystal frequency is the basic internal clock frequency of the microcontroller which can run at specified maximum and minimum frequencies, typically 1MHz to 16MHz
- The clock frequency, f; the smallest interval of time within the Microcontroller is called the pulse - P time



Crystal or Ceramic Resonator Oscillator Circuit

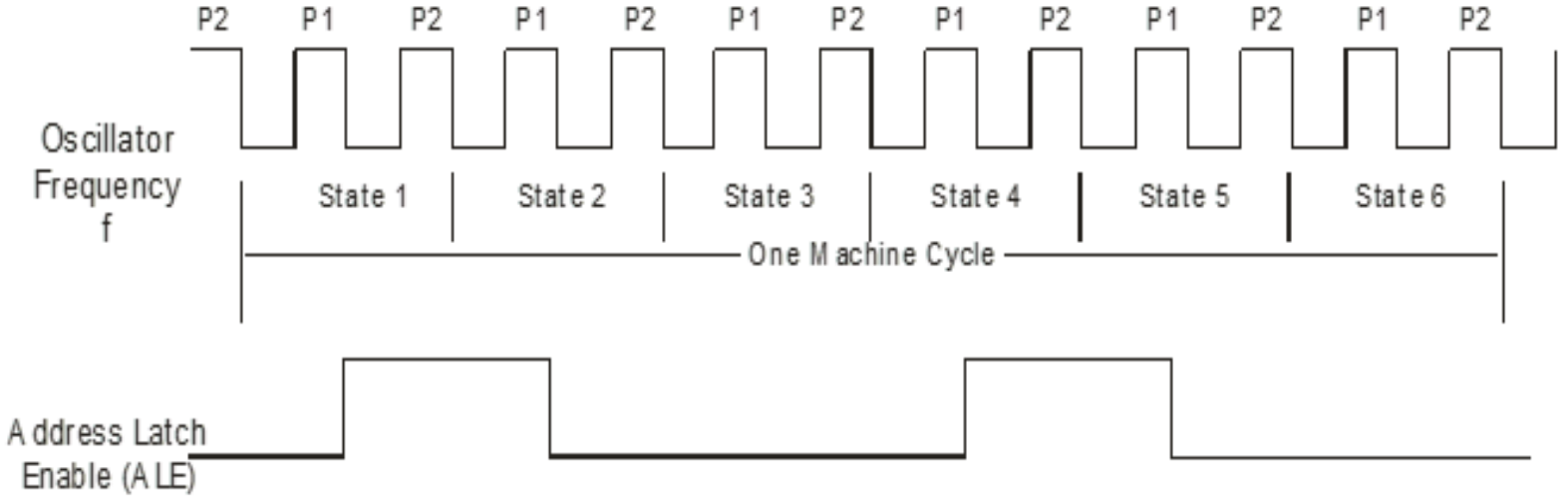


Image Source: https://codembedded.wordpress.com/

- A state is the basic time interval for discrete operations of the microcontroller, such as fetching an opcode, decoding an opcode, executing an opcode or writing a data byte
- Two oscillator pulses define each state
- The smallest interval of time to accomplish any simple instruction or part of a complex instruction, is known as the machine cycle
- The machine cycle is itself made up of 6 states
- Time taken by the instruction to execute is:

T_{inst} = (C x 12)/Crystal Frequency,

where C= no of Machine cycles

Ex:- f=16MHz, ADD A,R1 then

T_{inst} = (1 x 12)/16 M = 0.75 micro seconds

- There are 2 ALE pulses per machine cycle
- The ALE pulse, which is primarily used as a timing pulse for external memory access, indicates when every instruction byte is fetched
- 2 bytes of single instruction may thus be fetched and executed
- In one machine cycle, single byte instruction throw-away the second byte (which is the first byte of the next instruction)
- The next instruction is then fetched in the following cycle

Program Counter

- PC is a 16-bit register
- Which stores the address of next instruction to be executed
- The PC is automatically incremented after every instruction byte is fetched and may also be altered by certain instructions
- The PC is the only register that does not have an internal address

Data Pointer

- The DPTR register is made up of two, 8-bit registers, named as DPH and DPL
- DPTR is used to furnish memory addresses for internal and external code access and external data access
- The DPTR is under the control of program instructions and can be specified by its 16-bit name, DPTR or by each individual byte name DPH and DPL

A, B and CPU Registers

- The 8051 contains 34 general purpose registers, two of these registers are A and B
- A & B hold results of many instructions, particularly mathematical and logical operations
- The other 32 are arranged as part of internal RAM in 4 banks, B0 to B3; 8 registers in each bank
- The Accumulator register (A) is the most versatile of the two CPU registers and is used for many operations including addition, subtraction, multiplication, division and Boolean bit manipulations
- It is also used for all data transfer between the 8051 and any external memory
- The B register is used with A register for multiplication and division operations and has no other function other than as a location where data may be stored

Flags and the Program Status Word (PSW)

- Flags are 1-bit registers provided to store the results of certain program instructions
- Other instructions can test the condition of the flags and make decisions based on the flag states
- The 8051 has 4 math flags that respond automatically to the outcomes of math operations
- And 3 general purpose user flags that can be set to 1 or cleared to 0 by the programmer as desired
- The 4 math flags include Carry Flag (C), Auxiliary Carry Flag (AC), Overflow Flag (OV) and Parity Flag (P)
- The 3 user flags are designated as User Flag Zero (F0), Register Bank Select Bit-0 (RS0) and Register Bank Select Bit-1 (RS1)

```
MOV A,#35h      SETB PSW.4
```

- These flags are bit addressable as PSW.0 to PSW.7

CY	AC	F0	RS1	RS0	OV	–	P

1101 1001
1110 1101
1 1 0 0 0 1 1 0

CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1.
RS0	PSW.3	Register Bank selector bit 0.
OV	PSW.2	Overflow flag.
–	PSW.1	User-definable bit.
P	PSW.0	Parity flag. Set/cleared by hardware each instuction cycle to indicate an odd/even number of 1 bits in the accumulator.

R0,R1,R2.....R7

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

Internal Memory

- A functioning computer must have RAM and ROM memories
- RAM memory for variable data that can be altered as the program runs
- ROM memory for program code bytes
- Additional memory can be added externally using suitable circuits
- Internal circuitry access the correct memory based on the nature of the operation in progress

Internal RAM

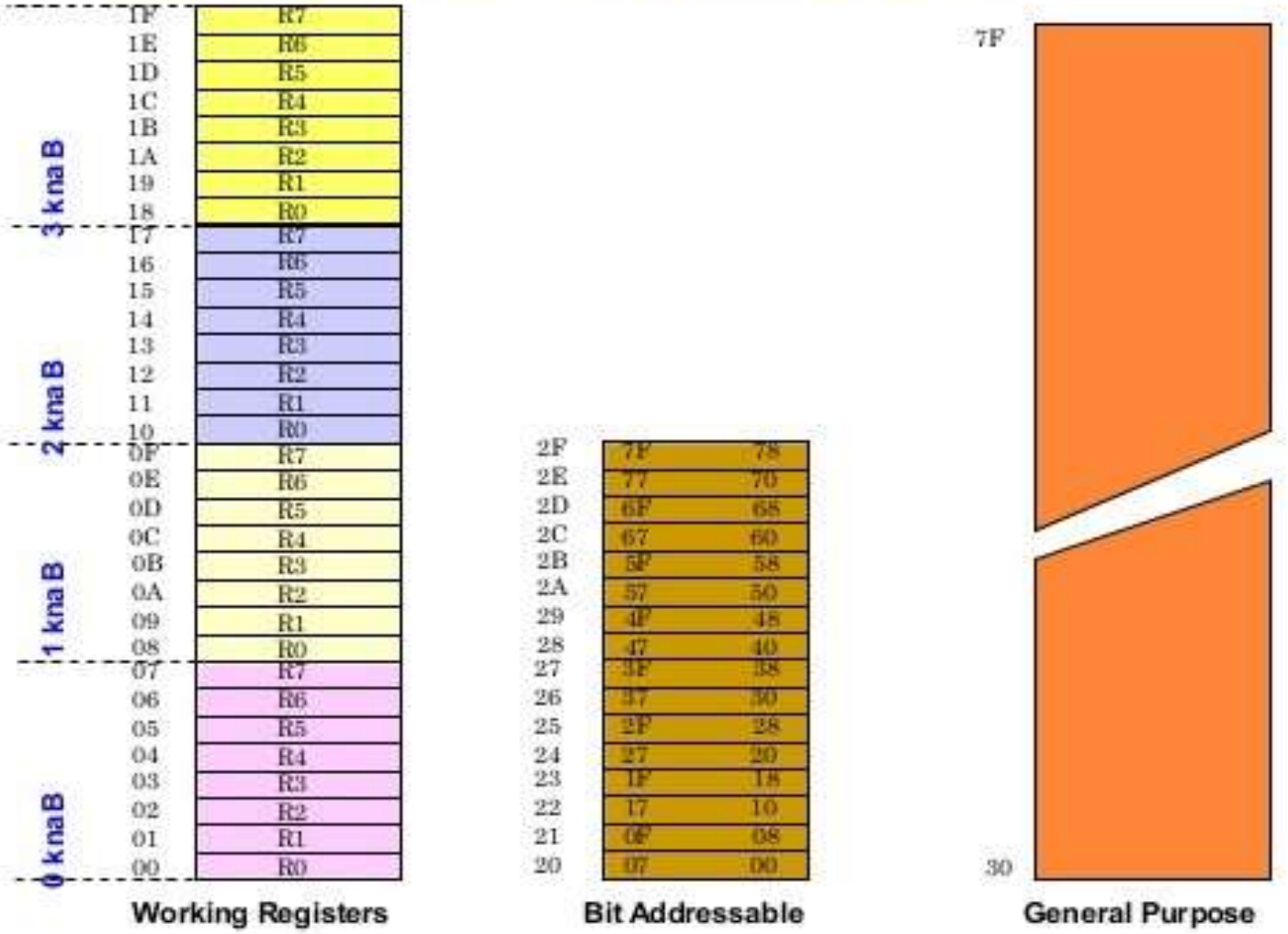
- 32 bytes from address 00h to FFh that make-up 32 working registers organized as 4 banks of 8 registers each
- The 4 banks are numbered 0 to 3 and are made- up of 8 registers named R0 to R7
- Each registers can be addressed by name or by its RAM address
- Bits RS0 and RS1 in the PSW determine which bank of registers is currently in use at any time when the program is running
- Register banks not selected can be used as general purpose RAM, Bank -0 is selected on reset
- A bit addressable area of 16 bytes occupies RAM byte addresses 20h to 2Fh forming a total of 128 addressable bits
- An addressable bit may be specified by its bit address of 00h to 07h or 8-bits may form any byte address from 20h to 2Fh
- A general purpose RAM area above the bit area from 30h to 7Fh addressable as byte

The Stack and The Stack Pointer

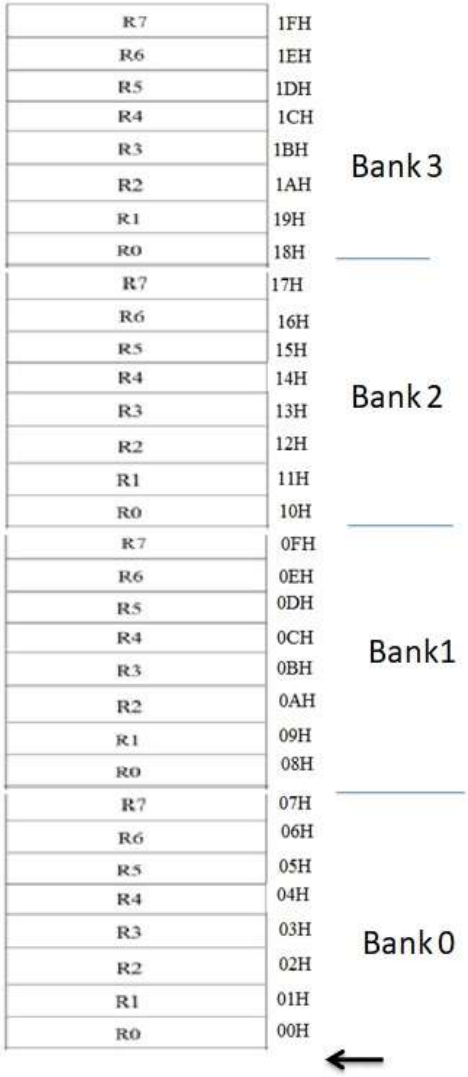
- The stack refers to an area of internal RAM that is used in conjunction with certain opcodes to store and retrieve data quickly
- The 8-bit stack pointer (SP) register is used by the 8051 to hold an internal RAM address that is called the top of the stack
- The address held in the SP register is the location in internal RAM where the last byte of data was stored by a stack operation
- When data is to be placed on the stack, the SP increments before storing data on the stack so that the stack grows up as data is stored

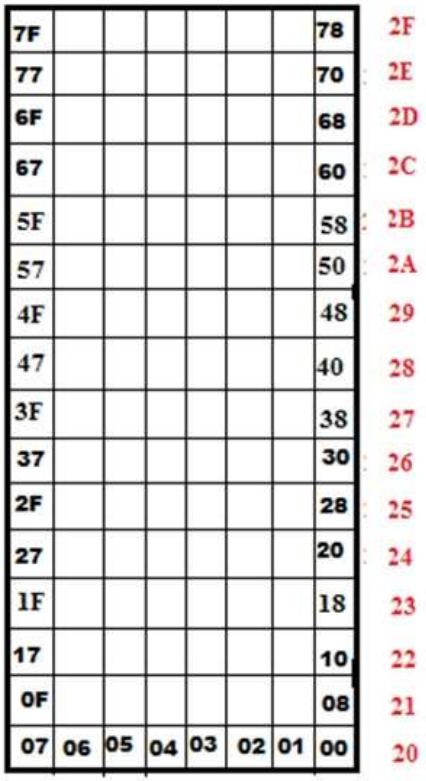
- As data is retrieved from the stack, the byte is read from the stack, and then the SP decrements to point to the next available byte of stored data
- The SP is set to 07h when the 8051 is reset and can be changed any internal RAM address by the programmer
- The stack is limited in height to the size of the internal RAM
- The stack has the potential to overwrite valuable data in the register banks, bit addressable RAM and scratch-pad RAM area
- The programmer is responsible for making sure the stack data does not grow beyond predefined bound

8051 Internal RAM Organisation



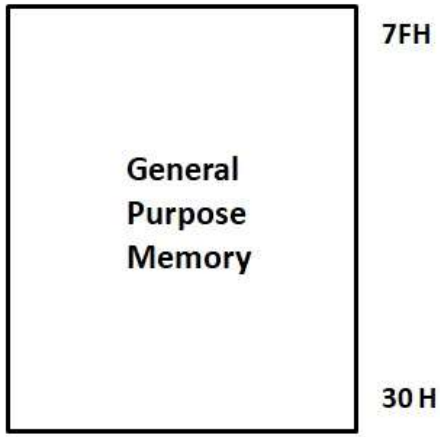
RAM Depicting Bit Addressable Area





Bit/Byte addressable memory area

SETB 20h
MOV 20h,#35h
MOV 20h,c



Special Function Registers

- SFR are a group of specific internal registers, which may be addressed much like internal RAM, using addresses from 80h to FFh
- SFRs are named in certain opcodes by their functional names, such as A, B, TH0 etc..
- Also referred by other opcodes by their addresses, such as 0E0h, 0F0h, 8Ch,80h,90h etc..
- Any address used in the program must start with a number

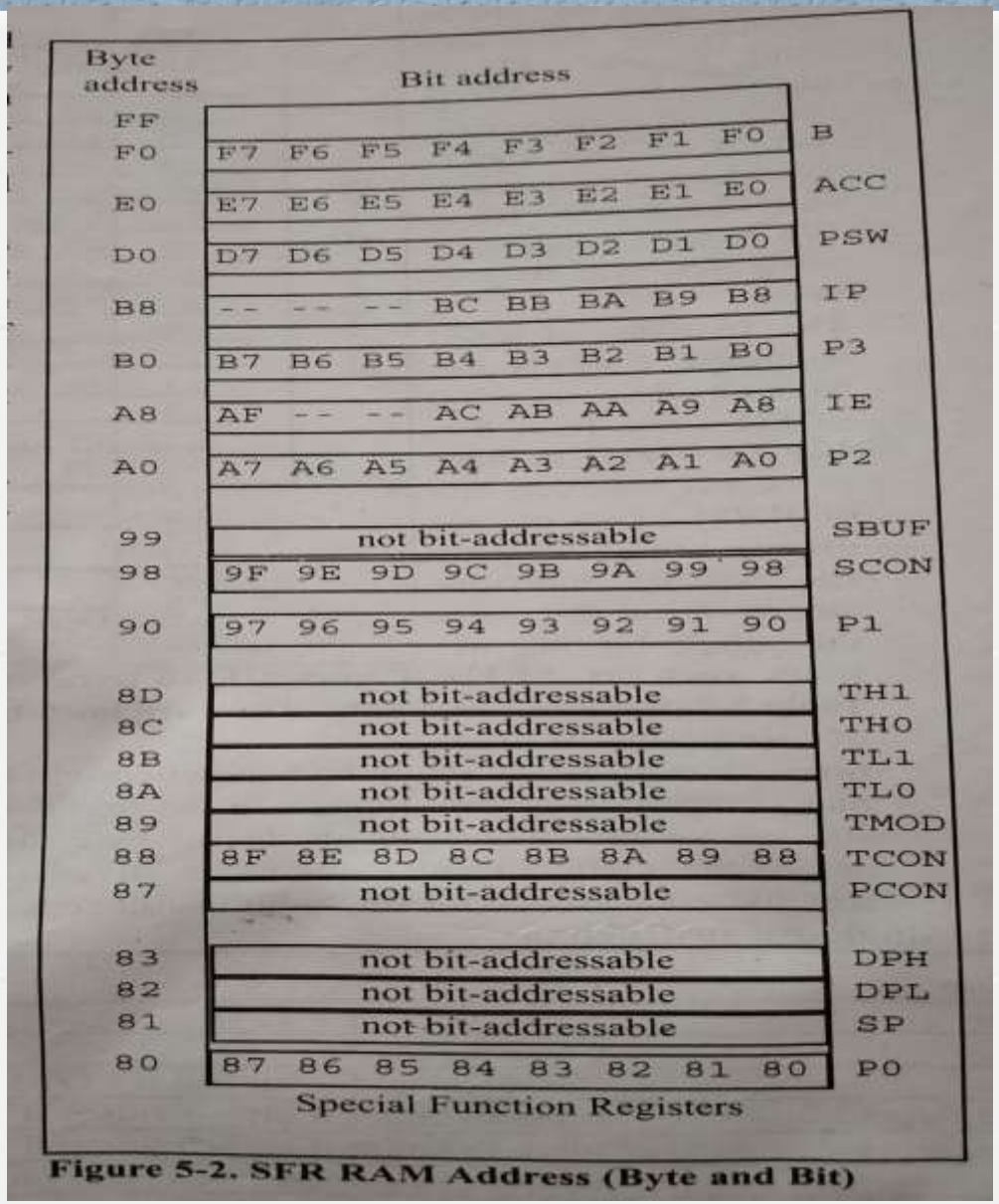


Figure 5-2. SFR RAM Address (Byte and Bit)

Special Function Registers

F8								FF
F0	B							F7
E8								EF
E0	ACC							E7
D8								DF
D0	PSW							D7
C8								CF
C0								C7
B8	IP							BF
B0	P3							B7
A8	IE							AF
A0	P2							A7
98	SCON	SBUF						9F
90	P1							97
88	TCON	TMOD	TL0	TL1	TH0	TH1		8F
80	P0	SP	DPL	DPH			PCON	87

Bit-addressable Registers

Internal ROM

- It can be addressed from 0000h to 0FFFh (4K bytes)
- The PC is ordinarily used to address program code bytes from address 0000h to 0FFFh
- Program address higher than 0FFFh, which exceeds the internal ROM capacity will cause the 8051 to automatically fetch code bytes from external program memory
- Code bytes can also be fetched exclusively from an external memory addresses from 0000h to FFFFh by connecting the external access pin (31) to ground

Input/ Output Pins, Ports and Circuits

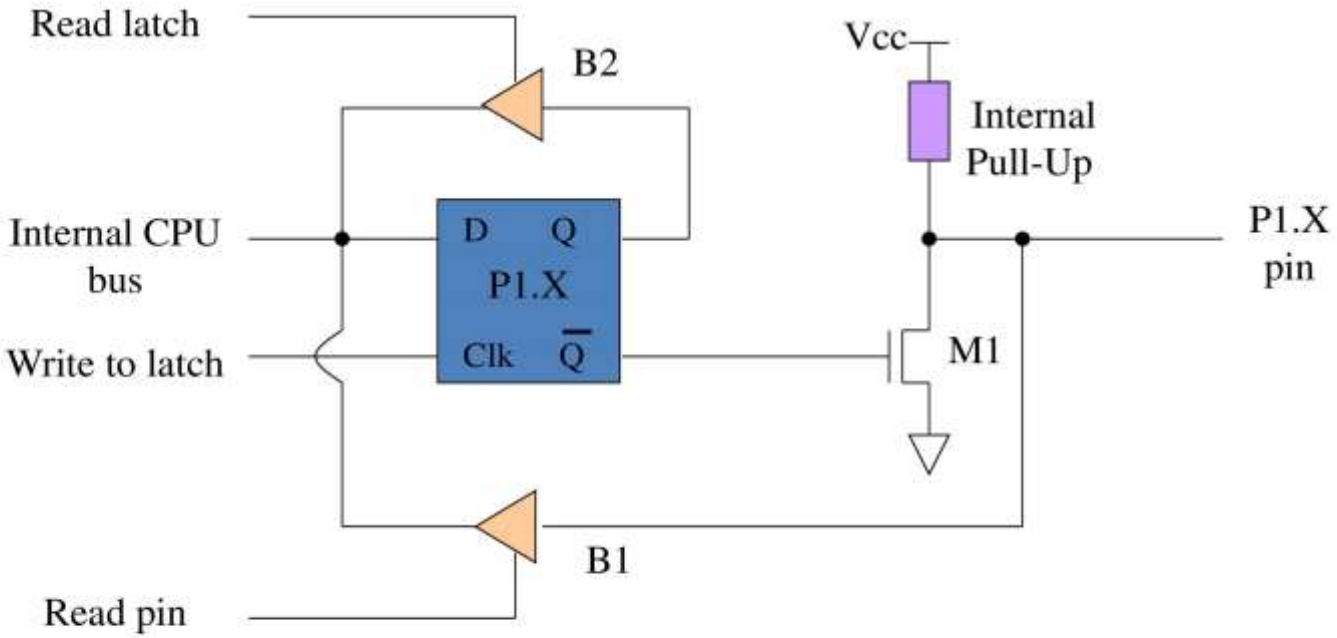
- 24 of the pins may each be used for one of two entirely different functions, yielding a total pin configuration of 64
- The function a pin performs at any given instant depends, first on what is physically connected to it and then on what software commands are used to “program” the pin
- Both of these factors are under the complete control of the 8051 programmer and circuit designer
- Each port has a D-type output latch for each pin
- The SFR for each port is made up of these 8 latches, which can be addressed as the SFR address for that port

Ex: the 8 latches for port 0 are addressed at location 80h,

Pin 3 of port 0 is the 2-bit of the P0 SFR – P0.2 (Px.y)

- The port latches should not be confused with the port pins; the data on the latches does not have to be the same as that on the pins
- The 2 data paths are shown in figure below by the circuits that read the latch or pin data using two entirely separate buffers
- The upper buffer is enabled, when latch data is read
- The lower buffer is enabled, when the pin state is read
- The status of each latch may be read from a latch buffer, while an input buffer is connected directly to each pin so that the pin status may be read independently of the latch state
- Different opcodes access the latch or pin status as appropriate port operations are determined by the manner in which the 8051 is connected to external circuitry
- Programmable port pins have completely different alternate functions.
- The configuration of the control circuitry between the output latch and the port pin determines the nature of any particular port pin function
- Among the 4 ports, port 1 cannot have alternate functions rest can be programmed

Hardware Structure of I/O Pin



ALU and Buses

- 8051 has 8-bit ALU, capable of performing arithmetic and logical operations 8-bit at a time
- 8051 has 8-bit data lines and 16-bit address lines
- EA!
- ALE
- PSEN!

Thank you